

Main BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
985-0052	PCBA,MLB_IG,DEV,J16	DEVELOPMENT,J16_DEVEL
639-4515	PCBA,MLB_IG,J16	J16,J16_COMMON,CPU:GOOD,SSD:Y,EEEE:FF3T
639-4704	PCBA,MLB_IG,BETTER,J16	J16,J16_COMMON,CPU:BETTER,SSD:Y,EEEE:FGWY
639-4705	PCBA,MLB_IG,CTO,J16	J16,J16_COMMON,CPU:CTO,SSD:Y,EEEE:FGY0

Bar Code Labels / EEEE #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7896	1	MLB LABEL, 2D	EEEE_FF3T	CRITICAL	EEEE:FF3T
825-7896	1	MLB LABEL, 2D	EEEE_FGY0	CRITICAL	EEEE:FGY0
825-7896	1	MLB LABEL, 2D	EEEE_FGWY	CRITICAL	EEEE:FGWY

BOM Groups

BOM GROUP	BOM OPTIONS
J16_COMMON	COMMON, ALTERNATE, J16_COMMON1, J16_COMMON2, J16_PROGPARTS
J16_COMMON1	XDP, SPEAKERID, TBTHV: P12V, CPUVCC: 3PHASE
J16_COMMON2	VDDQ: P1V35
J16_PROGPARTS	SMC: PROG, BOOTROM: PROG, T29ROM: PROG, CIVROM: PROG, CAMROM: PROG
J16_DEVEL	XDP_CONN, LPCPLUS, DDRVREF_DAC, DEVEL_SENSORS, DEVEL_AUDIO
DEVEL_SENSORS	AP_ISNS: Y, HDD_IVSNS: Y, TEMPSNSDEV
J16_PRODUCTION	AP_ISNS: N, HDD_IVSNS: N

ADD 'J16_PRODUCTION' AT REVA RELEASE

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4515	1	CRW,CRUZ,EU2.CO,2.7G,65W,4+3.1.15,4M,BGA	U0500	CRITICAL	CPU:GOOD
337S4516	1	CRW,CRUY,EU2.CO,3.0G,65W,4+3.1.13,4M,BGA	U0500	CRITICAL	CPU:BETTER
337S4517	1	CRW,CRUX,EU2.CO,3.2G,65W,4+3.1.3,6M,BGA	U0500	CRITICAL	CPU:CTO

ASIC Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4483	1	LYNX POINT MOBILE,C1,Q5,QE99,PCBG4695	U1100	CRITICAL	
338S1113	1	IC,TWT,CR-4C,B1,FWQ,C10,288 12X12 CP-FCB	U2800	CRITICAL	
33S0616	1	IC,BCM57766A,CIV+,A0,8X8	U3900	CRITICAL	
343S3908	1	IC,L8P561,LED BLKT CTLR,LLP24,B0-F	HL100	CRITICAL	

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S3783	1	IC, EFI, V0039, J16	U5210	CRITICAL	BOOTROM: PROG
335S0807	1	IC, 64 MBIT SPI SERIAL FLASH	U5210	CRITICAL	BOOTROM: BLANK
341S3781	1	IC, SMC, PROGRAMM, V2.12A30, J16	U5000	CRITICAL	SMC: PROG
338S1159	1	IC, SMC12-A3, 40MHZ/50MIPS, SCPL FW, 15780A	U5000	CRITICAL	SMC: BLANK
341S3734	1	IC, EEPROM, CR, V16, 2, J16	U2890	CRITICAL	T29ROM: PROG
335S0865	1	IC, EEPROM, SERIAL, 256KB, MLP8	U2890	CRITICAL	T29ROM: BLANK
341S3735	1	IC, ENET SPD, ROM, NIMONYX, V1.13, D7/D71	U3990	CRITICAL	CIVROM: PROG
335S0862	1	IC, SERIAL FLASH, 2MBIT, 2.7V, REV F	U3990	CRITICAL	CIVROM: BLANK
341S3778	1	IC, CAMERA, FLASH, V7229, J16	U4202	CRITICAL	CAMROM: PROG
335S0852	1	IC, FLASH, SPI, 1MBIT, 3V3	U4202	CRITICAL	CAMROM: BLANK

Schematic / PCB #'s


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-0164	1	SCH,MLB_IG,J16	SCH	CRITICAL	J16
820-3588	1	PCBF,MLB_IG,J16	PCB	CRITICAL	J16

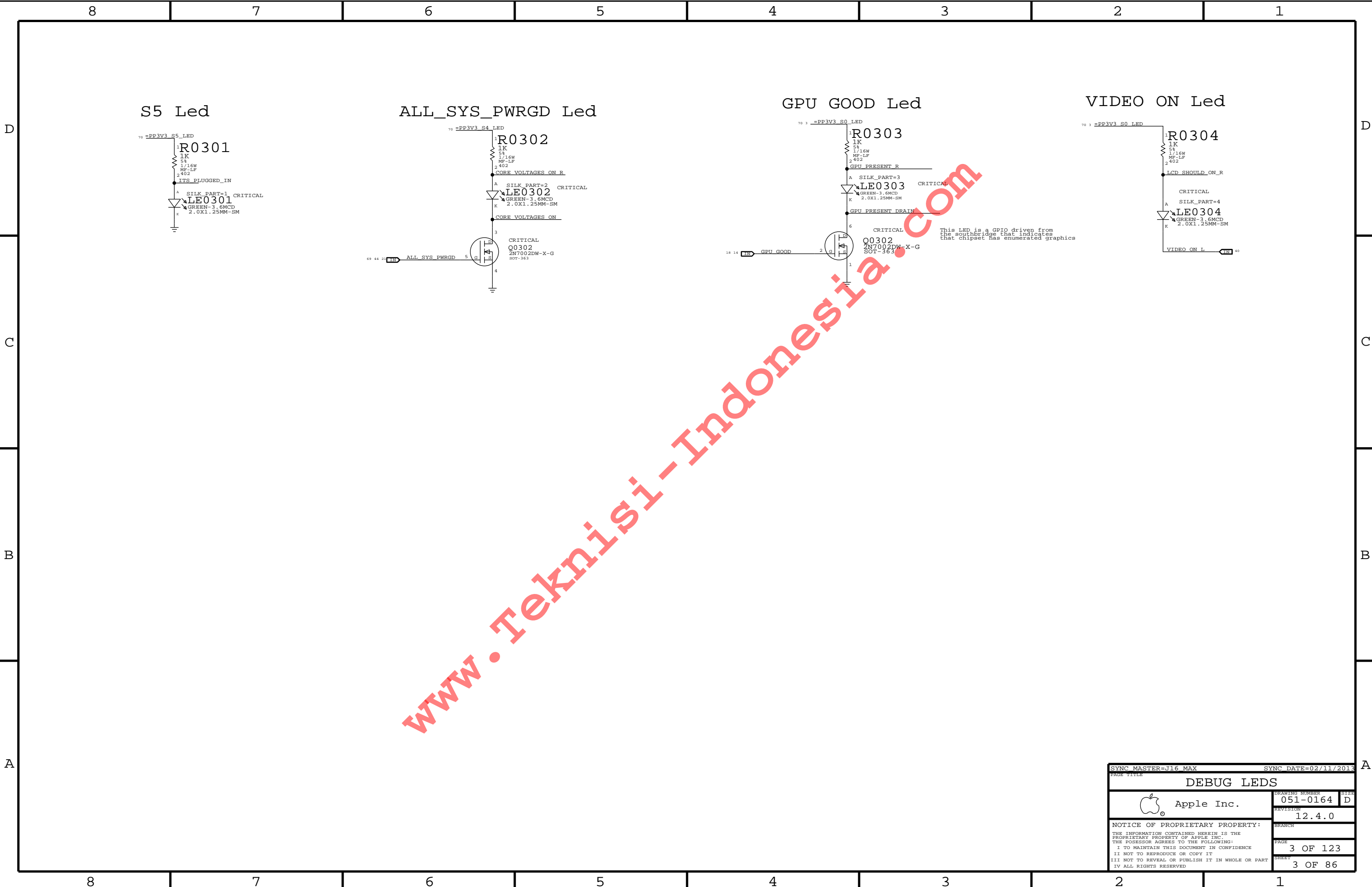
Alternates


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0147	377S0126		ALL	USB2 diodes
377S0155	377S0104		ALL	USB3 diodes
377S0124	377S0057		ALL	TVS
376S0975	376S1081		ALL	P/NCh dual FET
157S0084	157S0058		ALL	Enet magnetics
155S0578	155S0367		ALL	120OHM EMI BEAD
128S0368	128S0365		ALL	150UF AL POLY
138S0681	138S0638		ALL	Taiyo 10uF 805 al
197S0479	197S0478		Y4200	12 MHz Cam. Xtal
341S3747	341S3735		U3990	Enet ROM
107S0251	107S0249		ALL	Sense resistor
102S0880	102S0879		ALL	Sense resistor
197S0481	197S0480		ALL	25MHZ Xtal
138S0860	138S0775		ALL	Single-source 1uF 402
138S0859	138S0788		ALL	Single-source 10uF
138S0706	138S0739		ALL	Single-source 1uF 201

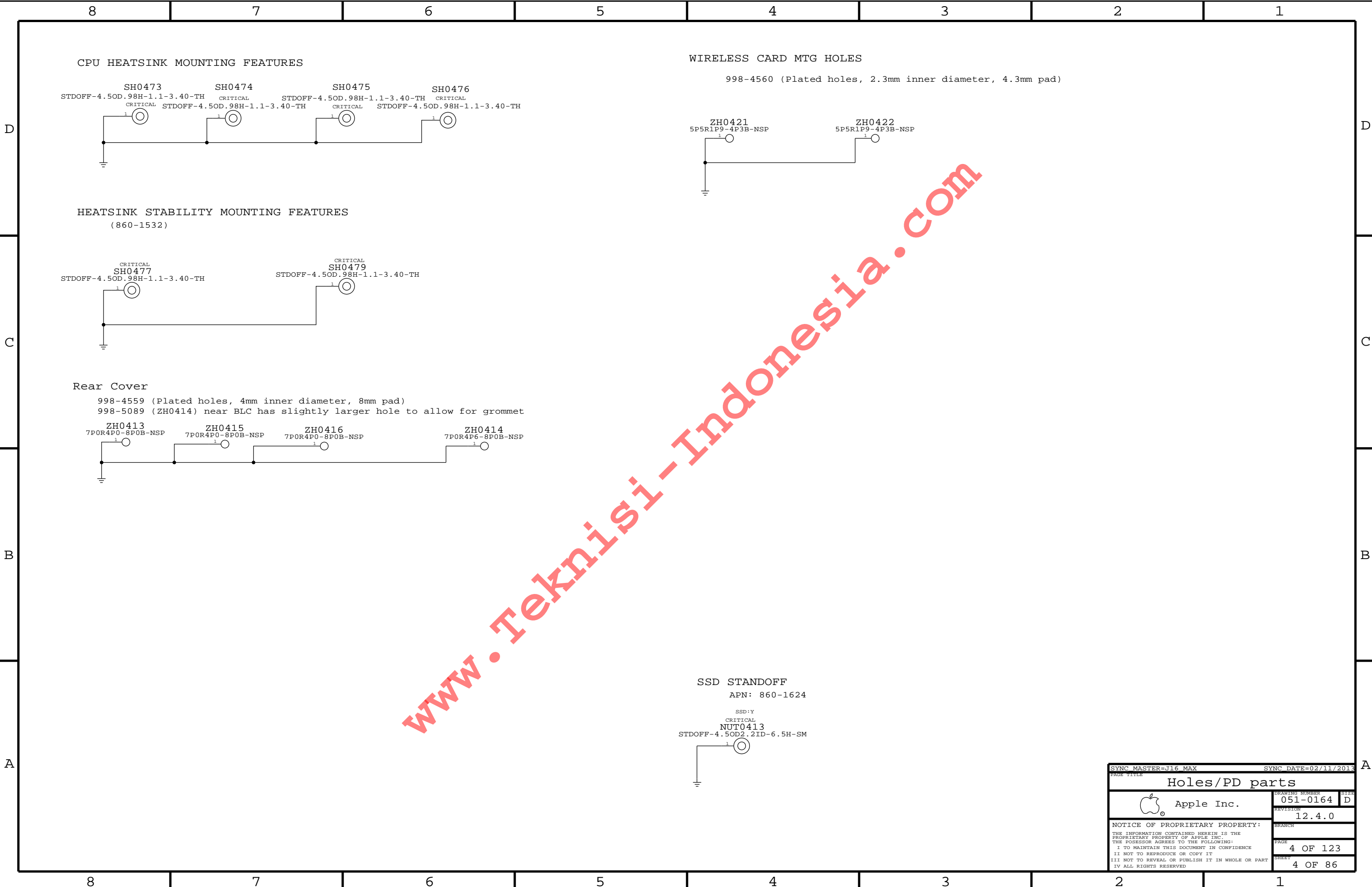
R5400, R5520, R5530


R5430

SYNCH MASTER=J16 DINI		SYNCH DATE=01/29/2013	
PAGE TITLE			
BOM Configuration			
	Apple Inc.		DRAWING NUMBER
			051-0164
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		REVISION	
		12.4.0	
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SYNC MASTER=J16 MAX		SYNC DATE=02/11/2013	
PAGE TITLE			
DEBUG LEDS			
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SYNC MASTER=J16 MAX		SYNC DATE=02/11/2013	
PAGE TITLE		Holes/PD parts	
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B

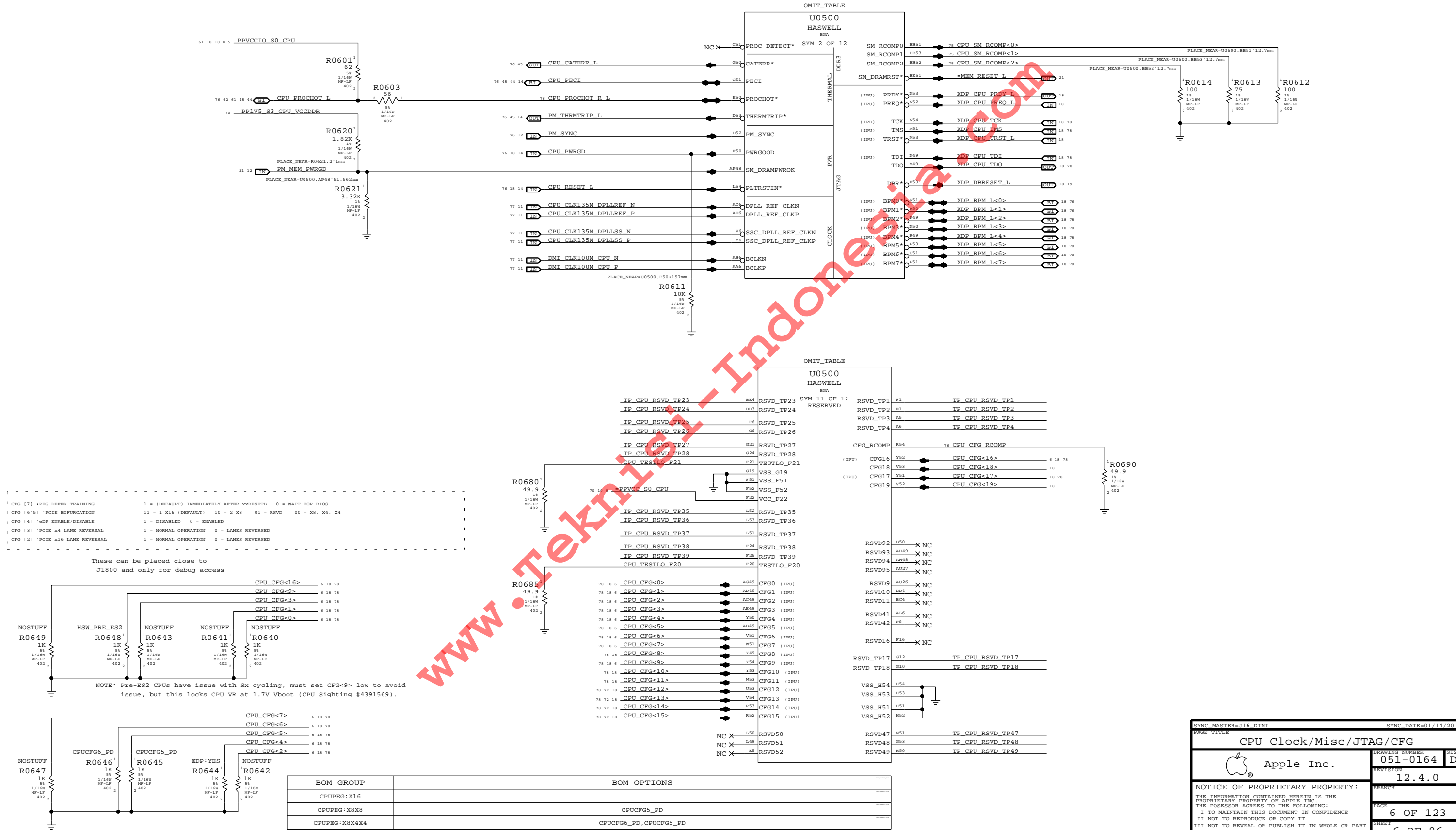
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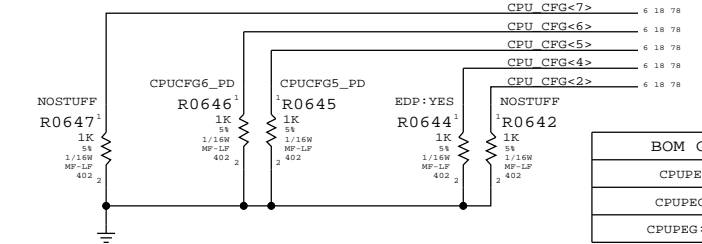
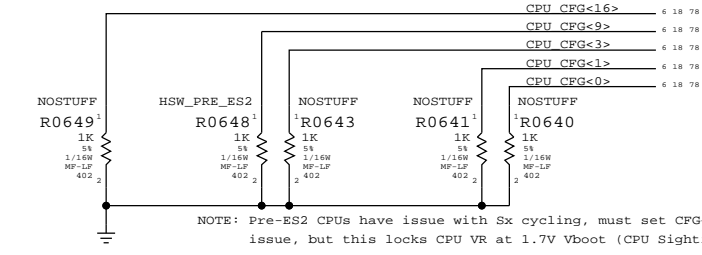
B

A



CFG [7] :PEG DEVER TRAINING 1 = ((DEFAULT)) IMMEDIATELY AFTER xRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED

These can be placed close to J1800 and only for debug access



BOM GROUP	BOM OPTIONS
CPUPEG:X16	
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD, CPUCFG5_PD

SYNC MASTER=J16 DINI

SYNC DATE=01/14/2013

CPU Clock/Misc/JTAG/CFG

Apple Inc.

DRAWING NUMBER 051-0164

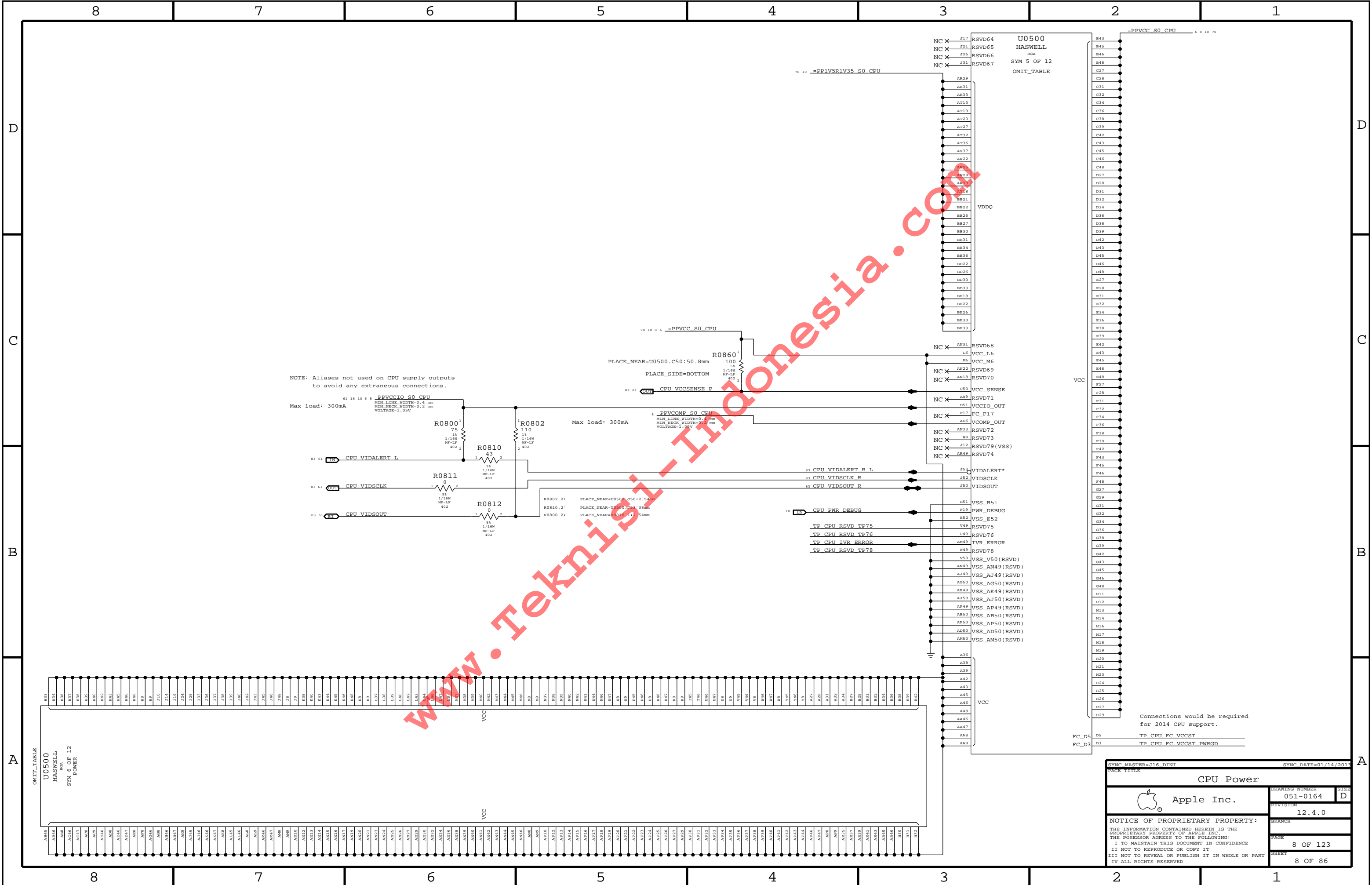
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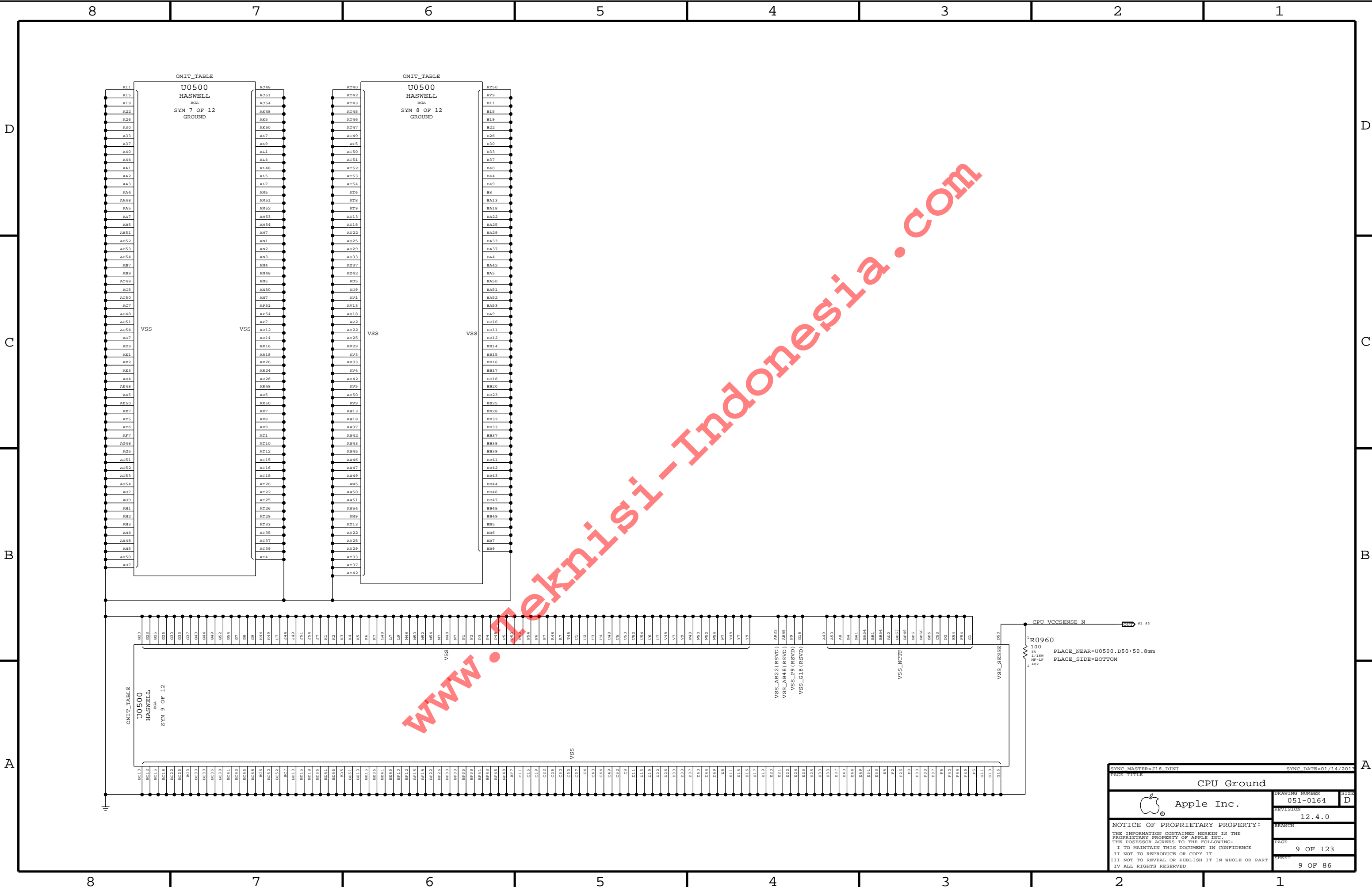
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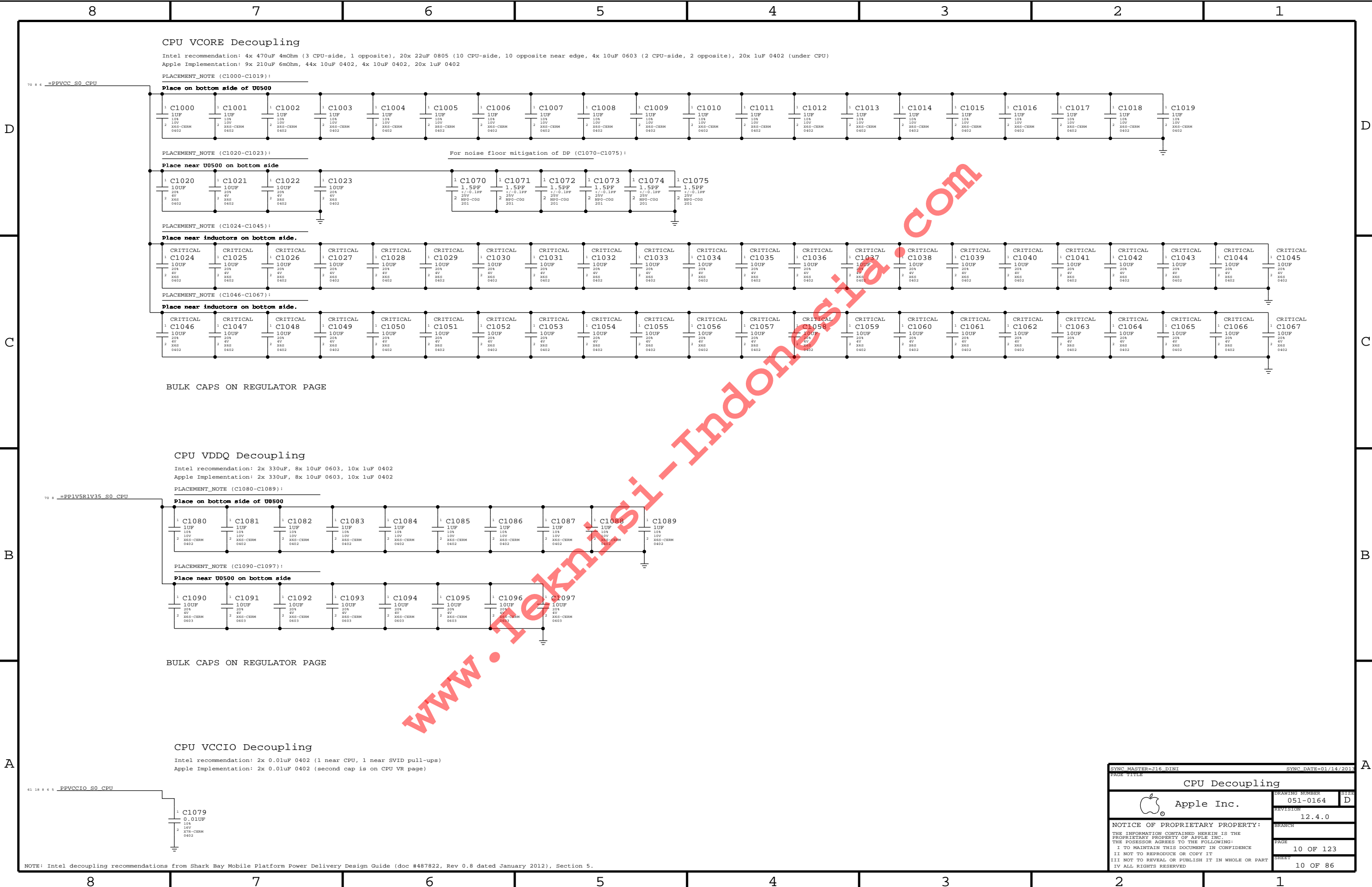
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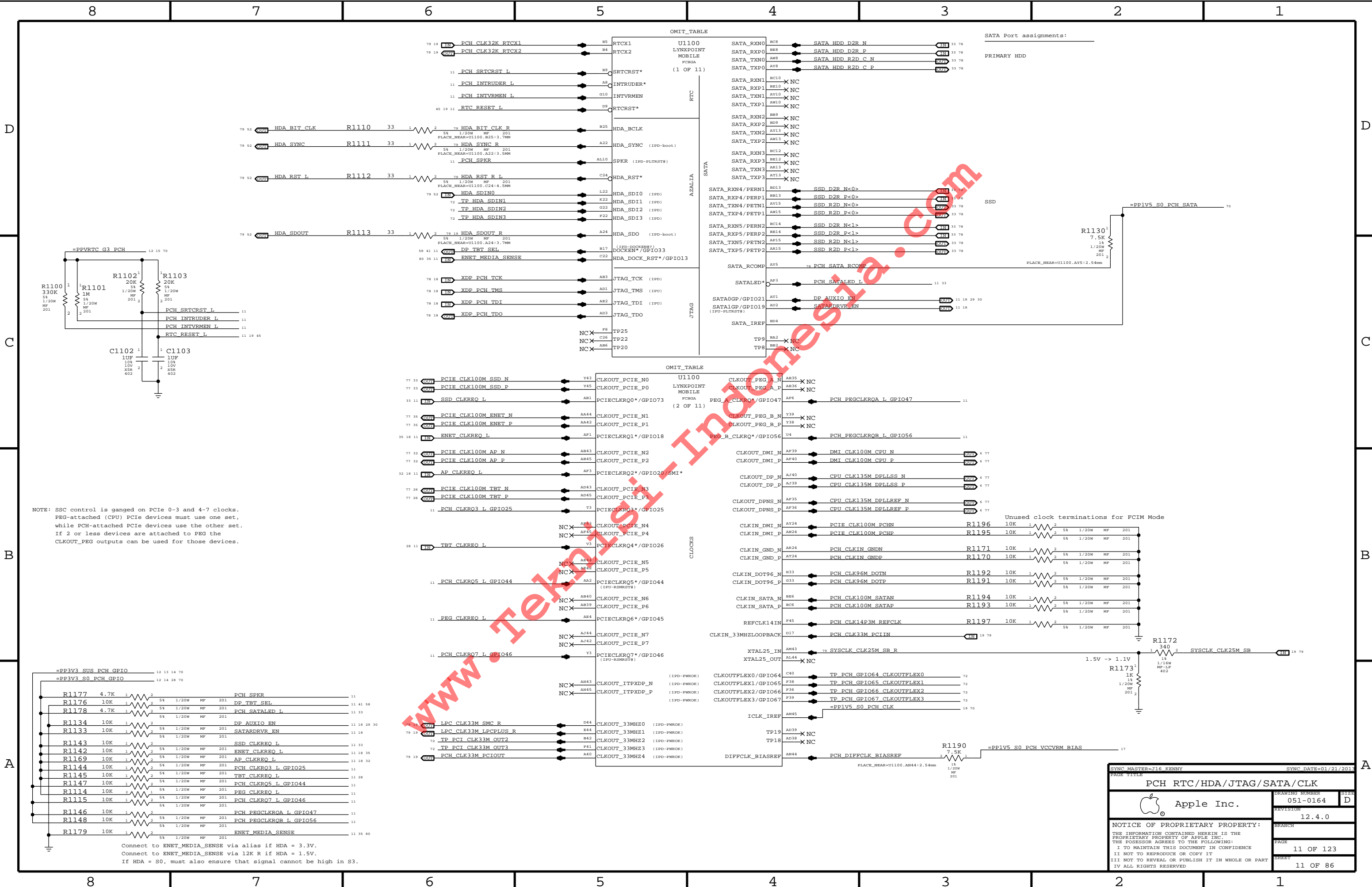
SYNC MASTER=J16 DINI		SYNC DATE=01/14/2013	
PAGE TITLE		CPU Power	
Apple Inc.		DRAWING NUMBER	051-0164
		REVISION	12.4.0
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PAGE TITLE			
CPU Ground			
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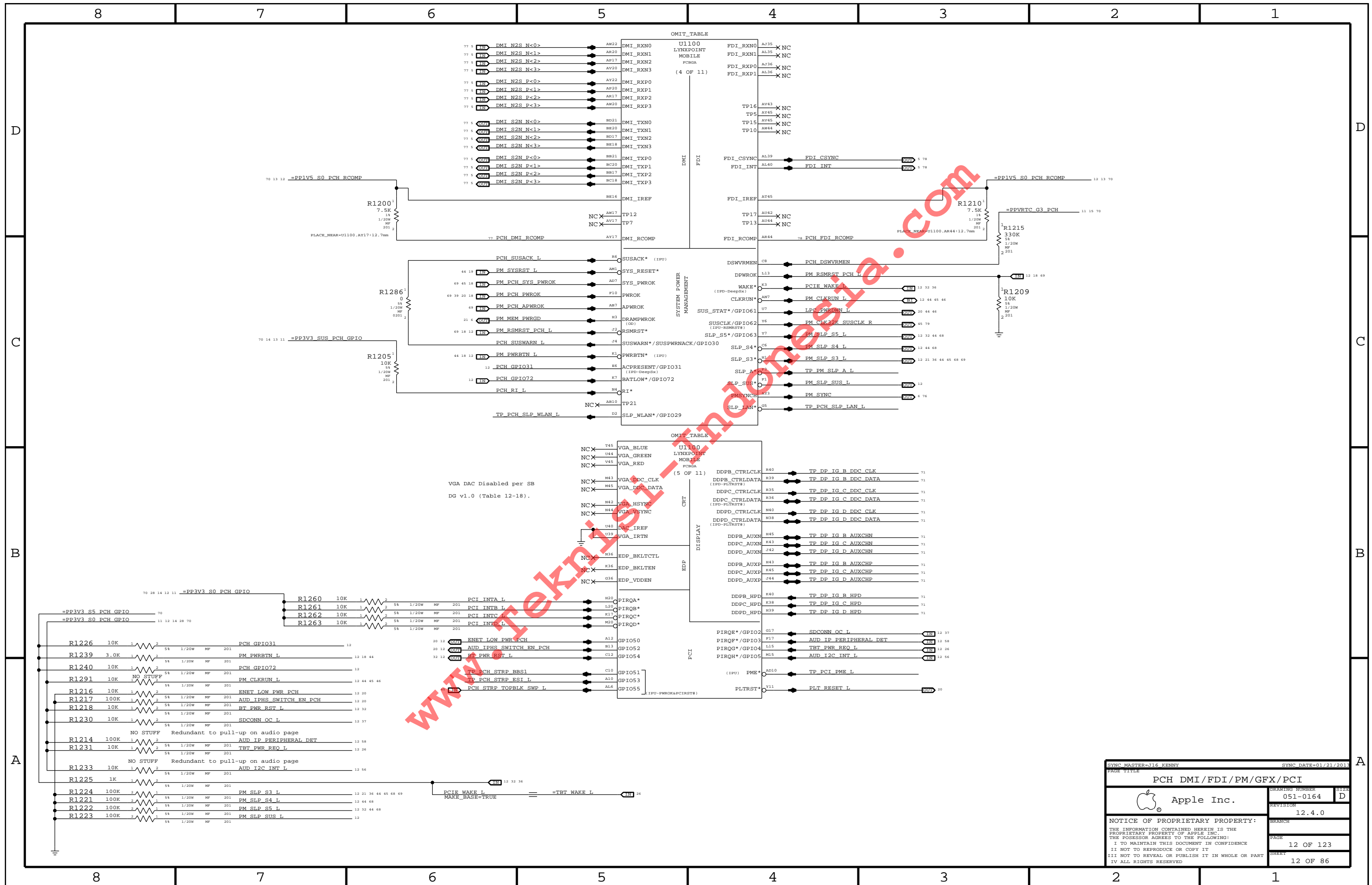


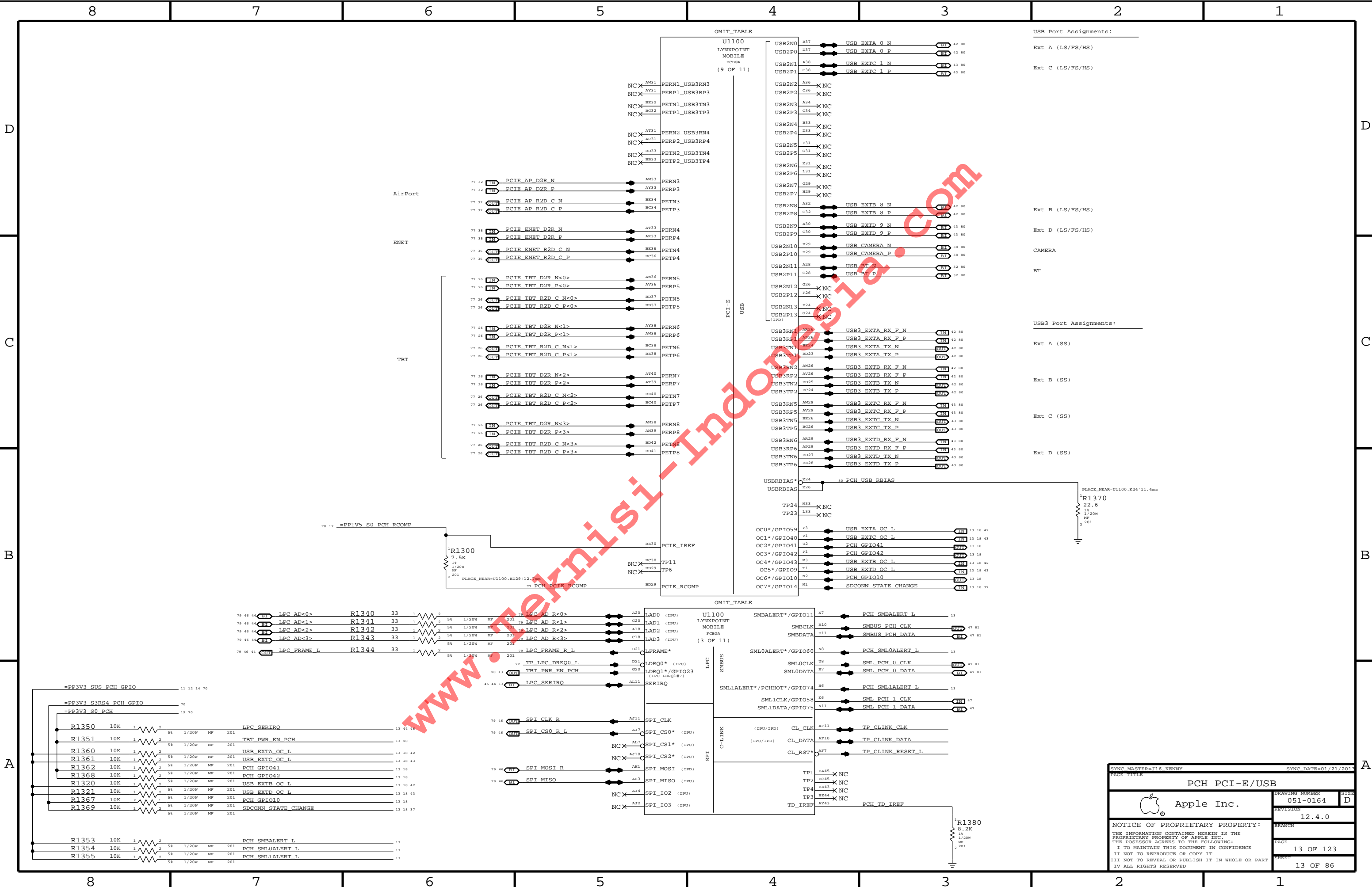
SYNC MASTER=J16 DINI		SYNC DATE=01/14/2013	
PAGE TITLE			
CPU Decoupling		DRAWING NUMBER	051-0164
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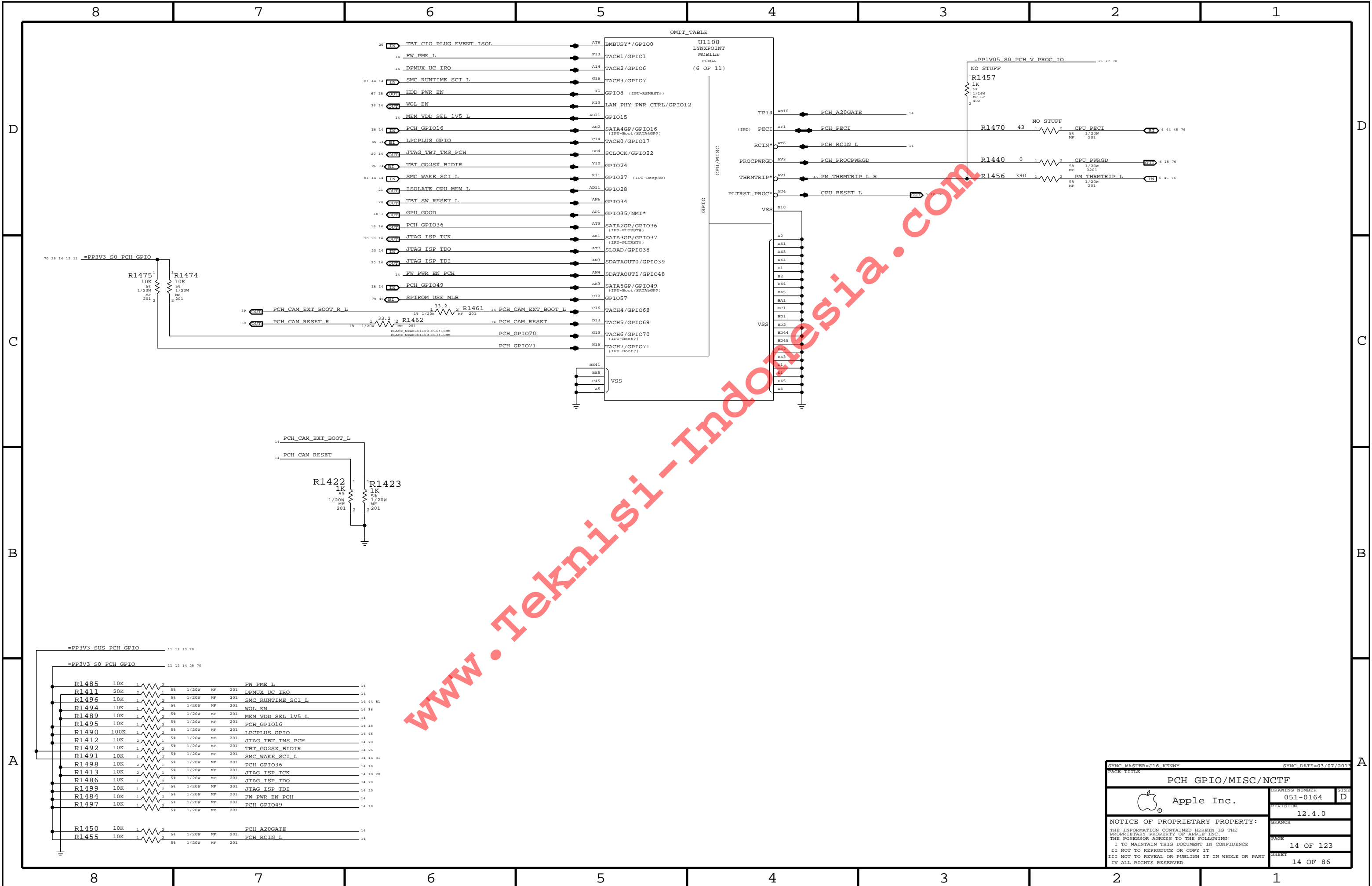


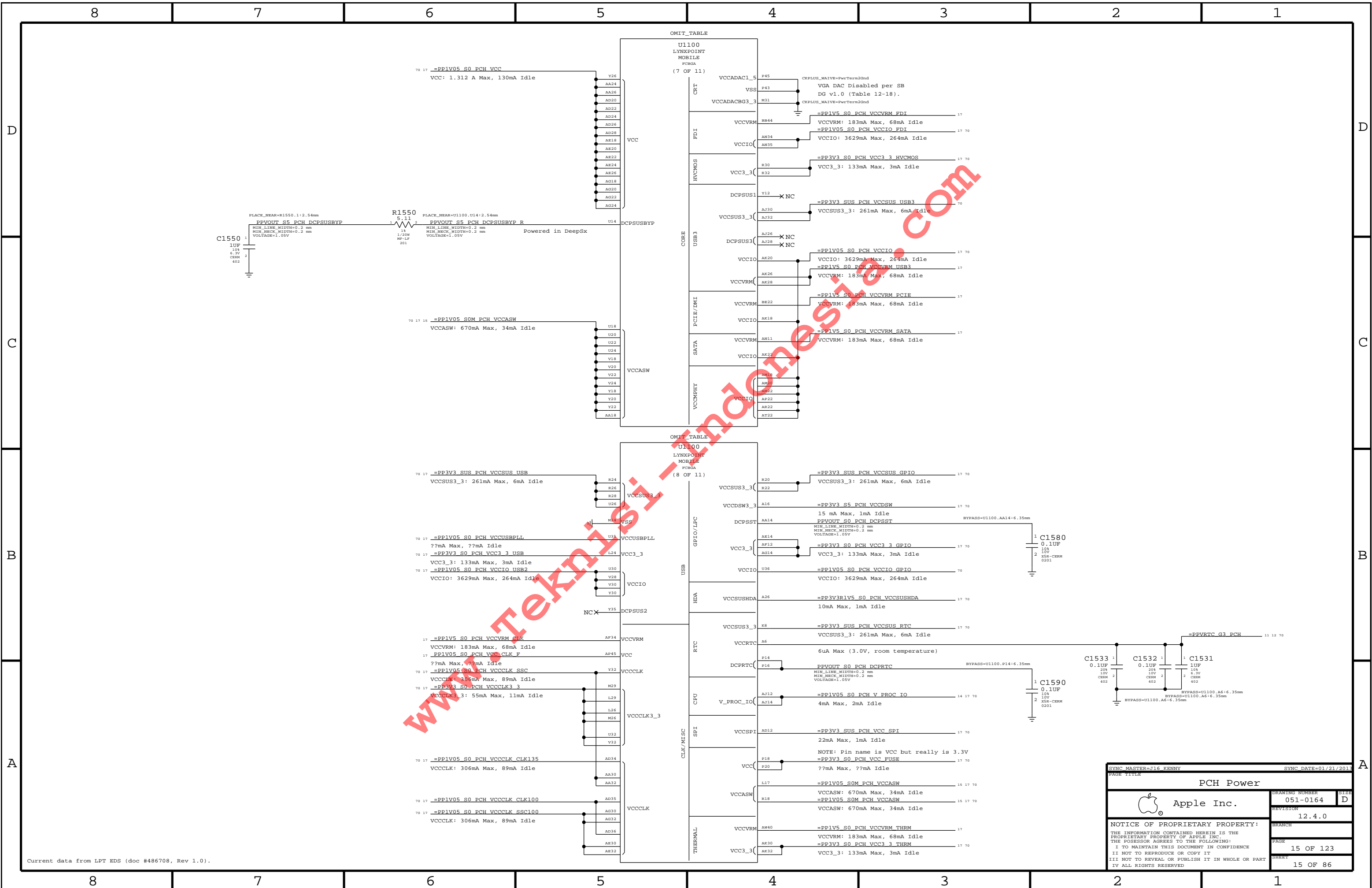
NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks.
PEG-attached (CPU) PCIe devices must use one set,
while PCH-attached PCIe devices use the other set.
If 2 or less devices are attached to PEG the
CLKOUT_PEG outputs can be used for those devices.

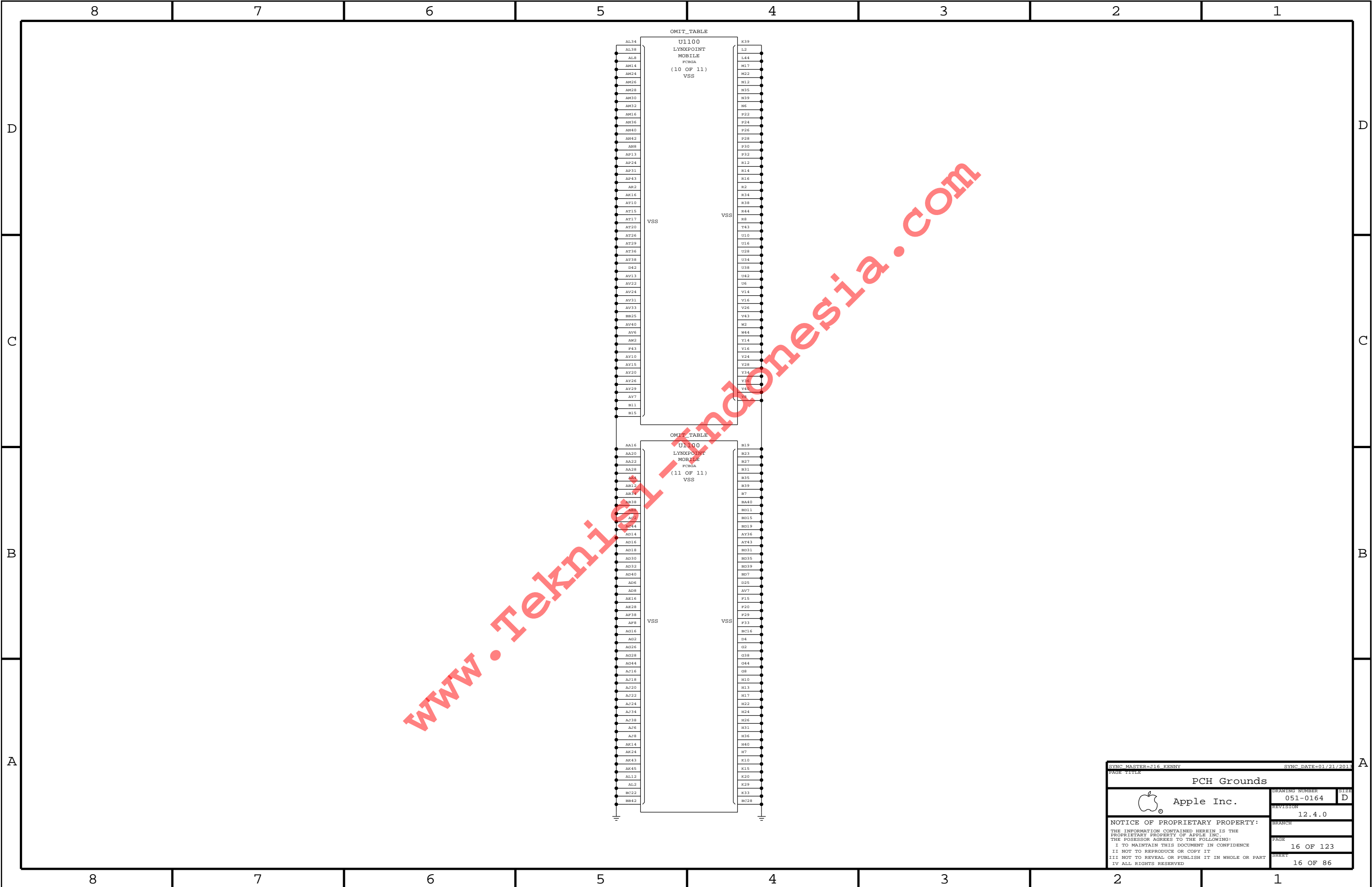
SYNC MASTER=J16 KENNY		SYNC DATE=01/21/2013	
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PCH RTC/HDA/JTAG/SATA/CLK			
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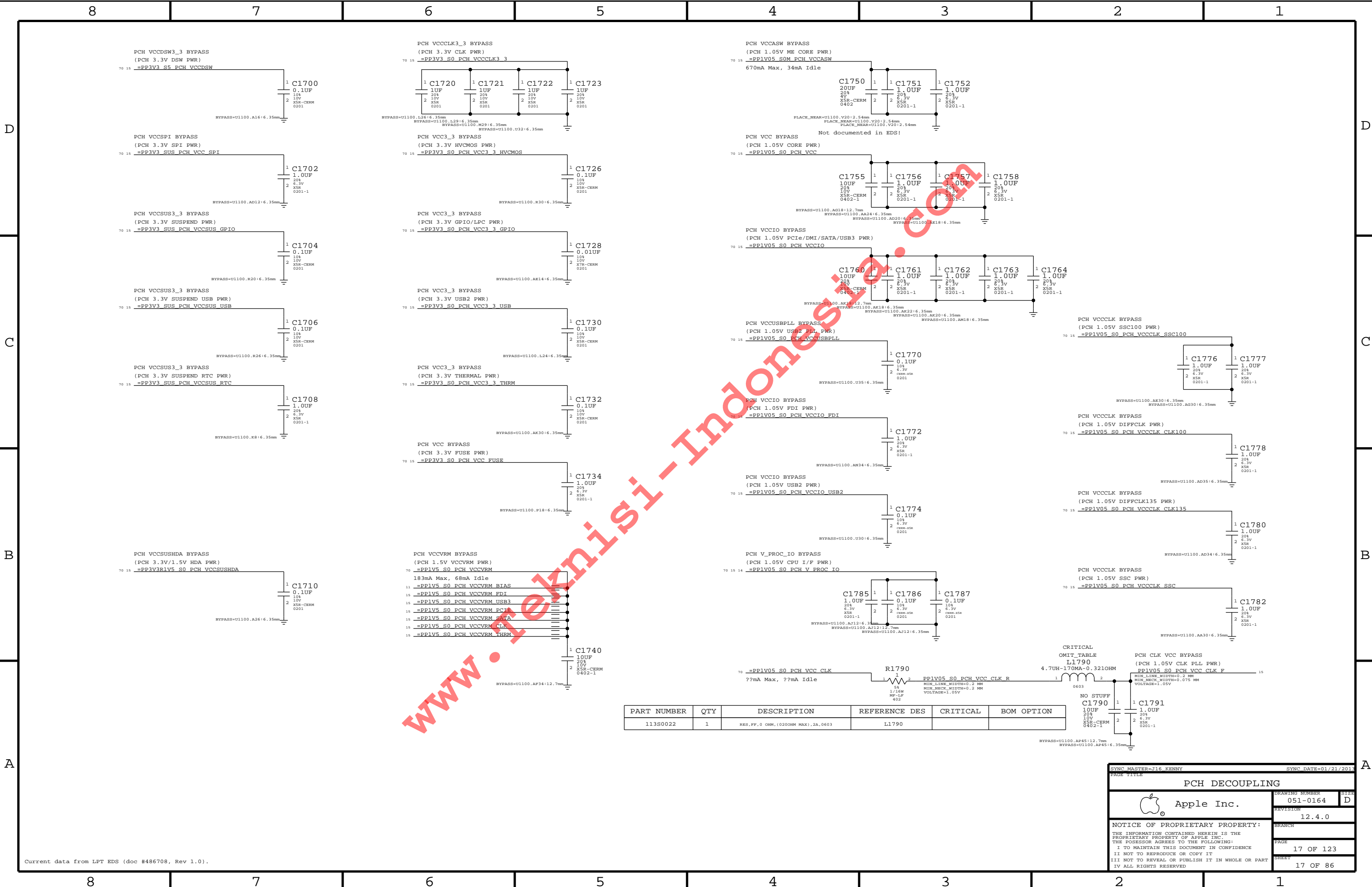













PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	1	RES,FP,0 OHM,(020OHM MAX),2a,0603	L1790		

SYNC MASTER=J16 KENNY

SYNC DATE=01/21/2013

PAGE TITLE

PCH DECOUPLING

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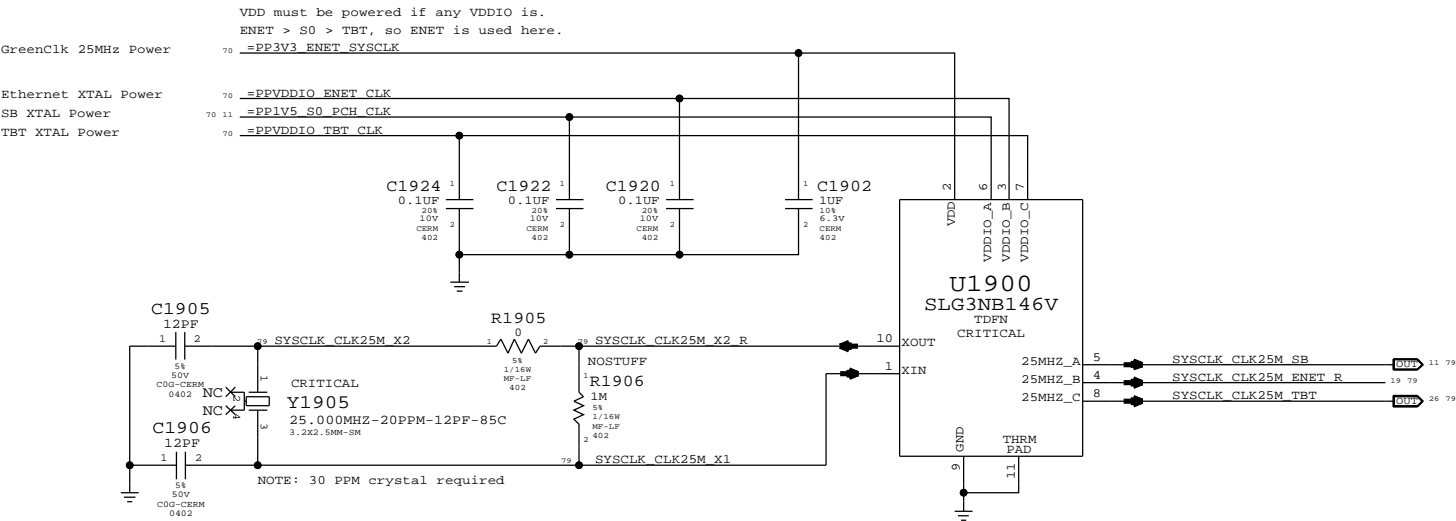
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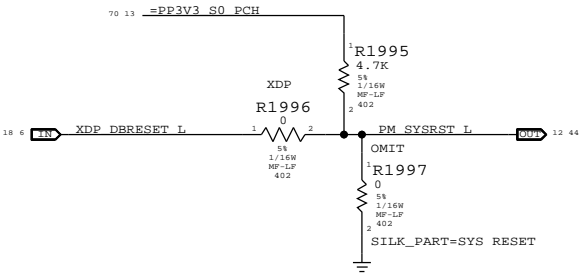
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Current data from LPT EDS (doc #486708, Rev 1.0).

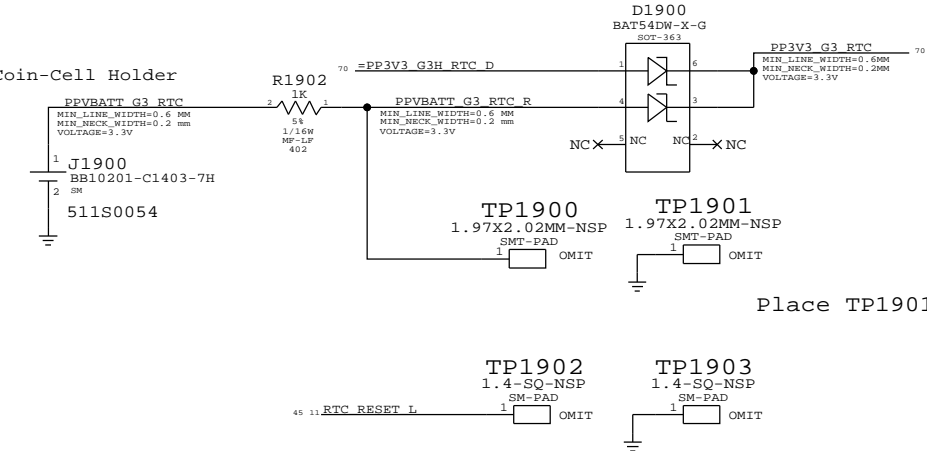
System 25MHz Clock Generator



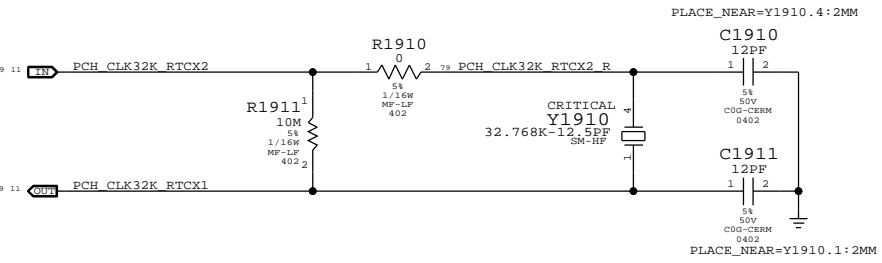
PCH Reset Button



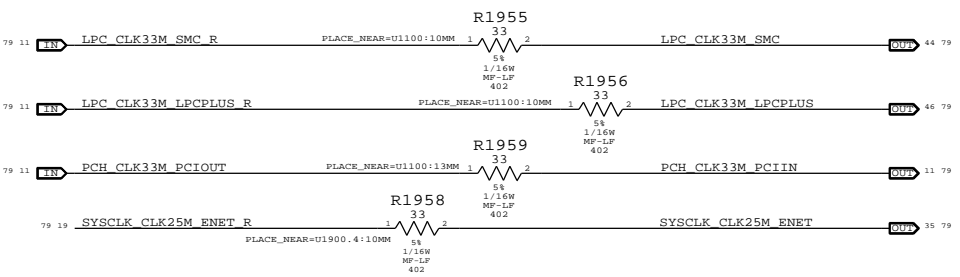
RTC Power Sources



PCH RTC Crystal

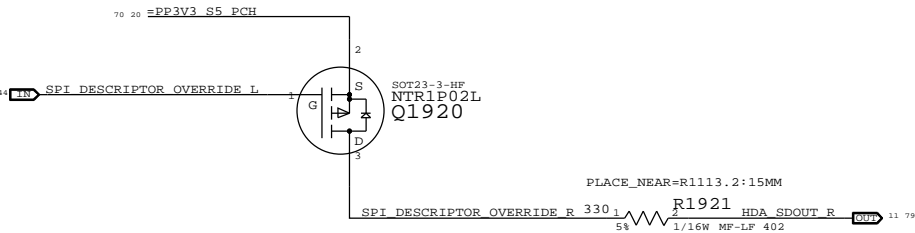



Clock series termination

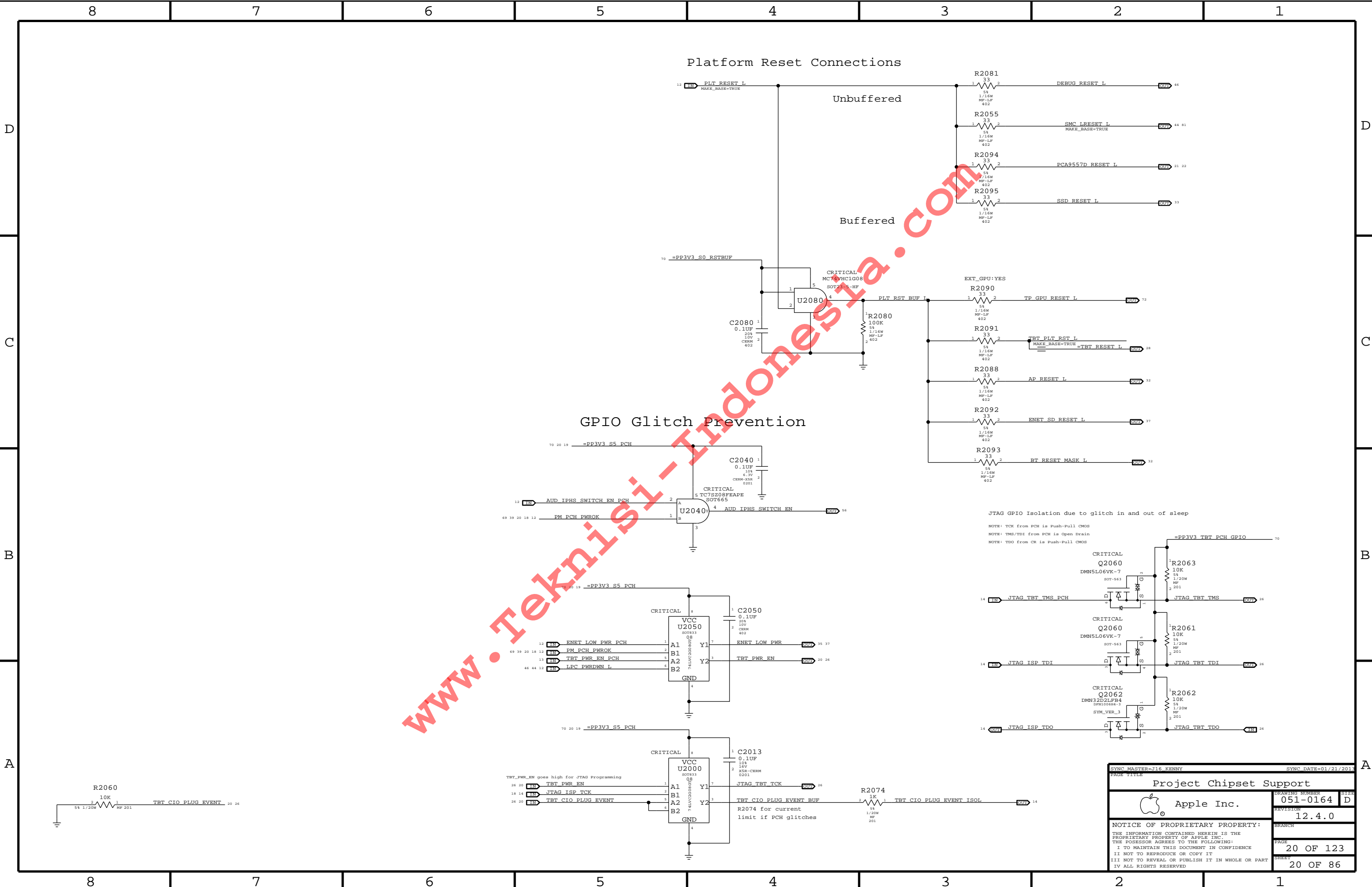


PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting.



SYNC MASTER=J16 KENNY		SYNC DATE=01/21/2013	
PAGE TITLE			
Chipset Support			
 Apple Inc.	DRAWING NUMBER	051-0164	SIZE D
	REVISION	12.4.0	
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SYNC MASTER=J16 KENNY

SYNC DATE=01/21/2013

PROJECT TITLE

Project Chipset Support

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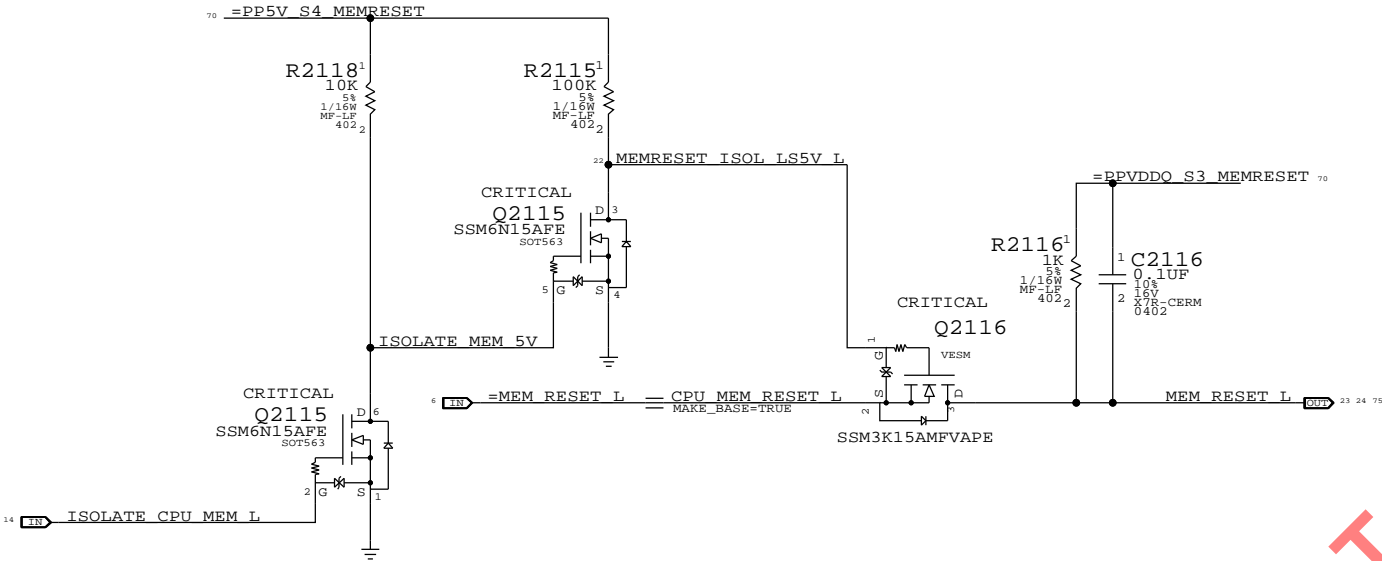
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals.

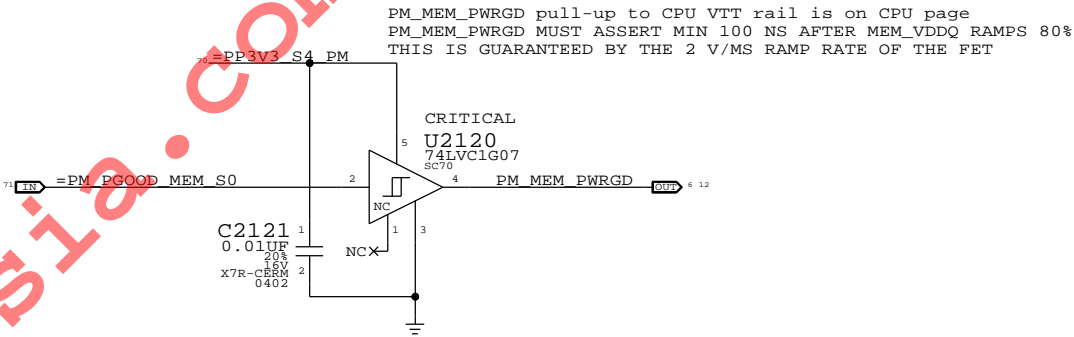
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

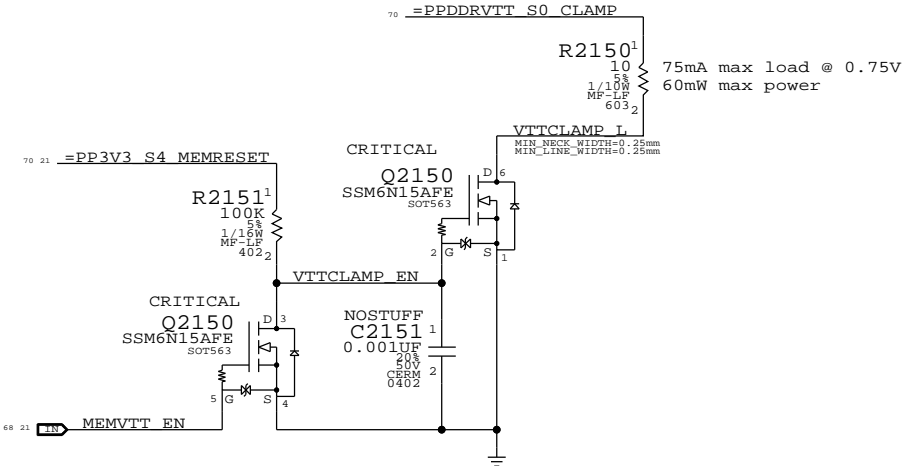
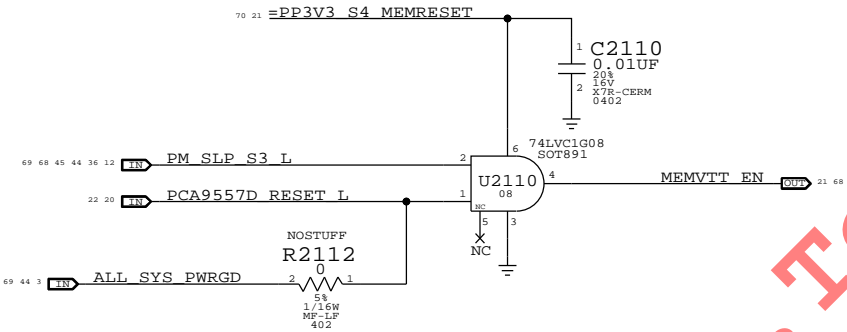
```
MEMVTT_EN = PLT_RESET_L * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L
```



MEM S0 "PGOOD" FOR CPU



MEMVTT Clamp
Ensures CKE signals are held low in S3



Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN
S0	0	1	1	1	CPU_MEM_RESET_L	1
to	1	0	1	1	1	1
2	0	0	1	1	1	0
3	0	0	0	X	1	0
S3	4	0	1	X	1	0
to	5	0	1	0 (*)	1	1
6	0	1	1	1	1	1
S0	7	1	1	1	CPU_MEM_RESET_L	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must de-assert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=J16 NICK

SYNC DATE=12/11/2012

CPU Memory S3 Support

Apple Inc.

051-0164

12.4.0

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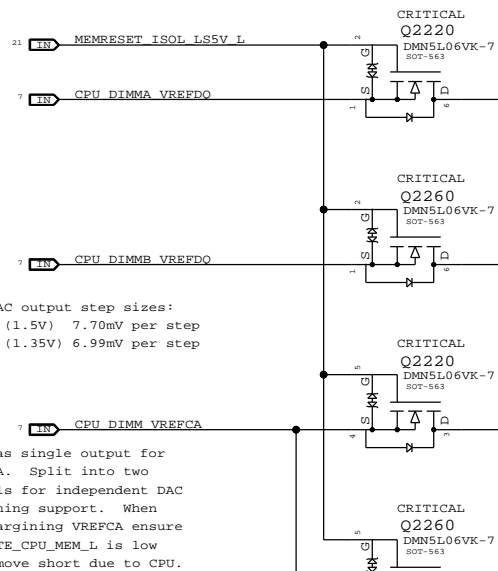
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during S3

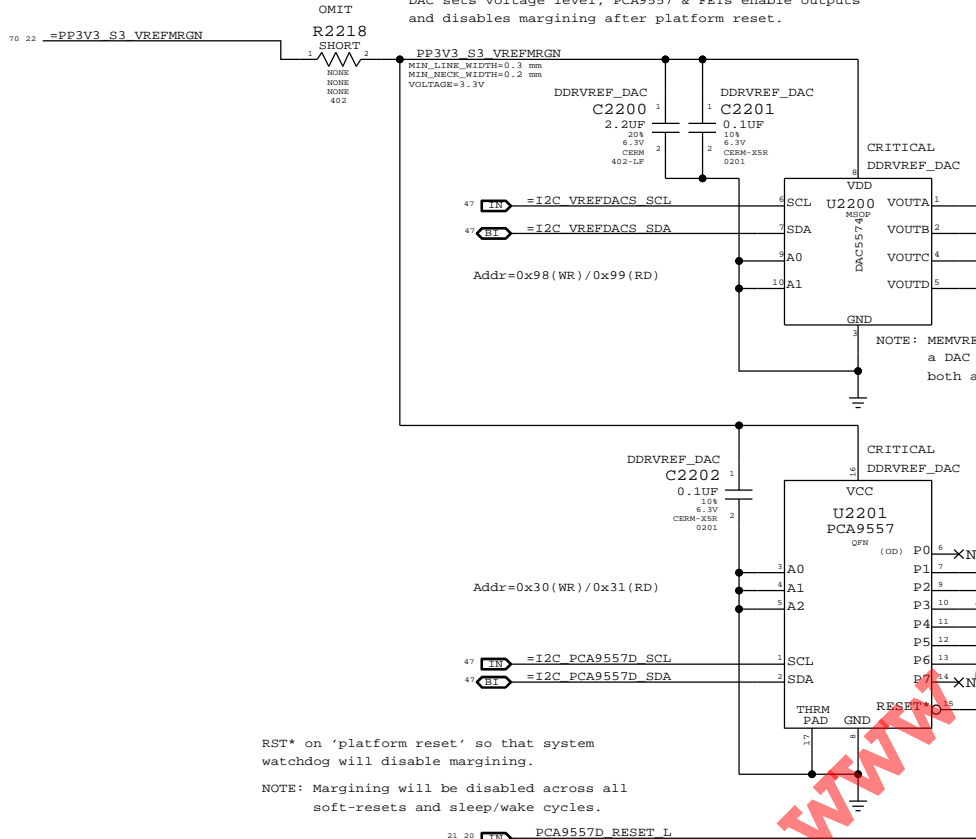


NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure ISOLATE_CPU_MEM_L is low to remove short due to CPU.

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.



RST* on 'platform reset' so that system watchdog will disable margining.

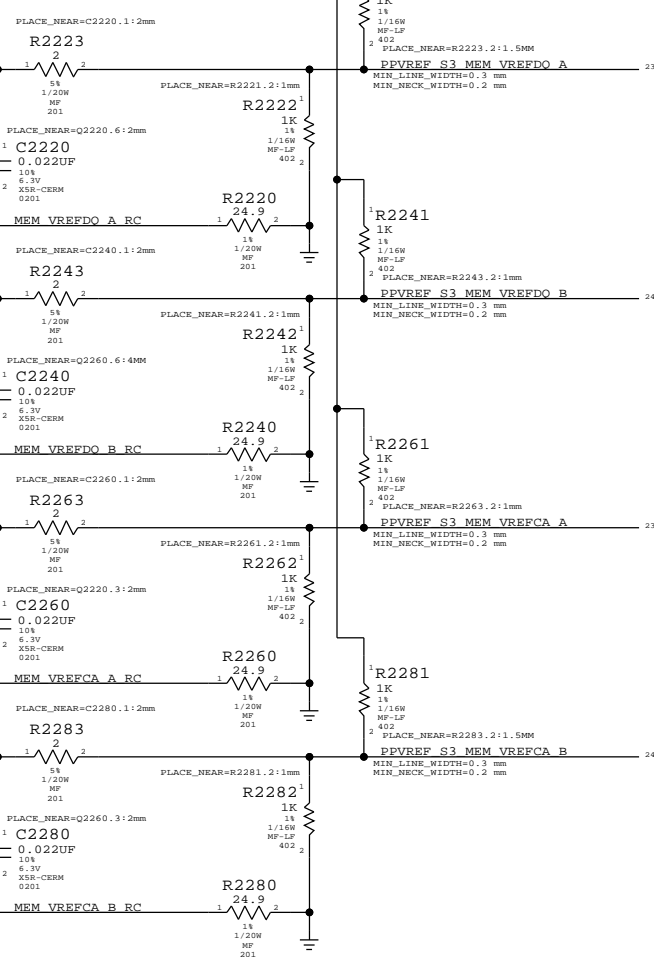
NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG
DAC Channel:	A	B	C	C	D
PCA9557D Pin:	1	2	3	4	5
	DDR3 (1.5V)		DDR3L (1.35V)		
Nominal value	0.750V (DAC: 0x3A = 0.747mV)		0.675V (DAC: 0x34 = 0.670mV)		1.500V (DAC: 0x74 = 1.495V)
Margined target:	0.300V - 1.200V (+/- 450mV)		0.275V - 1.075V (+/- 400mV)		1.200V - 1.800V (+/- 300mV)
DAC range:	0.000V - 1.508V (0x00 - 0x75)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 3.004V (0x00 - 0xE9)
Margined range:	0.299V - 1.206V (+/- 453mV)		0.269V - 1.083V (+/- 406mV)		0.932V - 1.760V (+/- 414mV)
VRef current:	+901uA - -911uA (- = sourced)		+811uA - -816uA (- = sourced)		+36uA - -36uA (- = sourced)
DAC step size:	7.68mV / step @ output		7.67mV / step @ output		2.575mV / step @ output

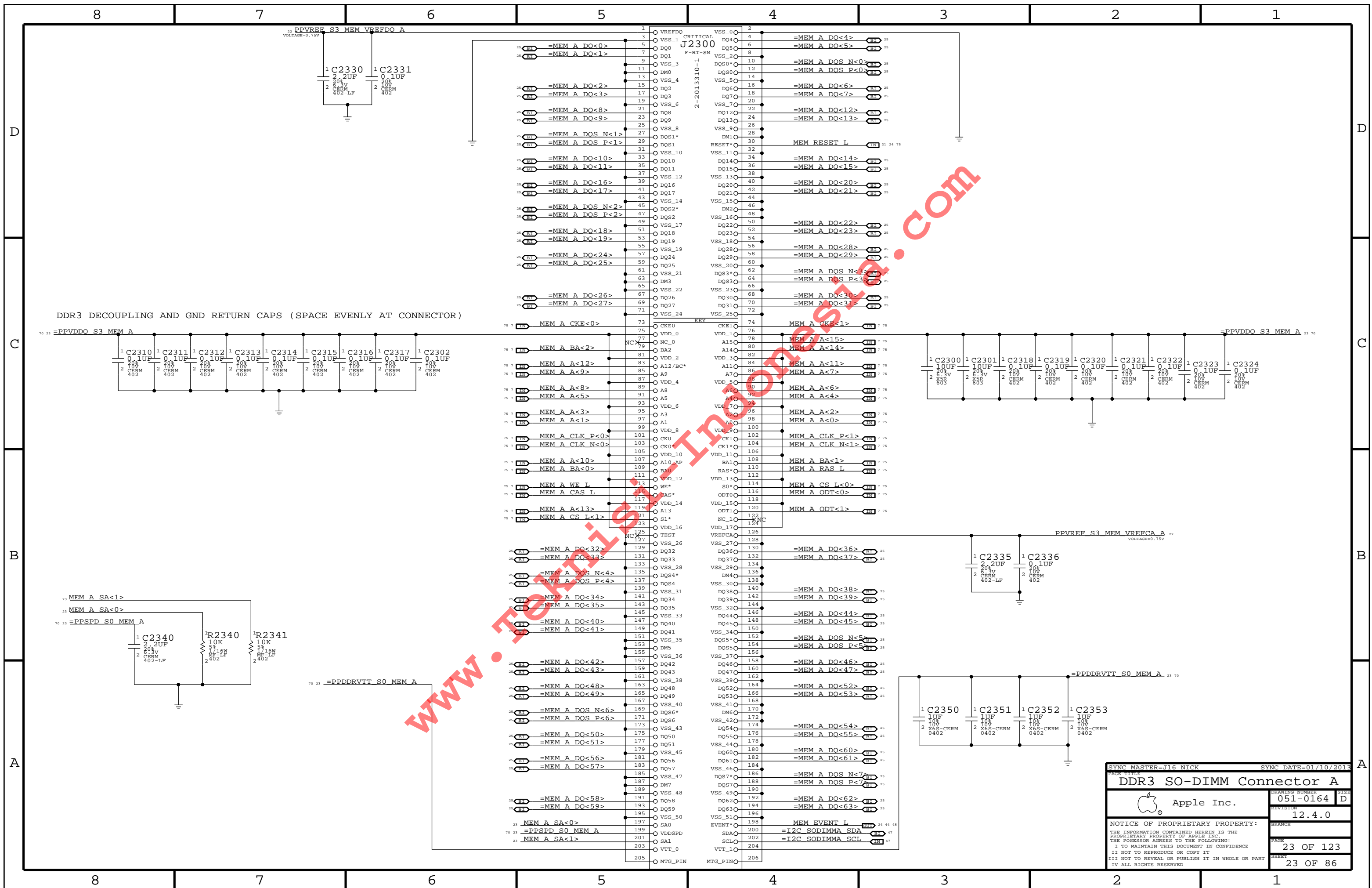
NOTE: DDR3 assumes TP51916 supply with 10.0k/49.9k divider
DDR3L assumes TP51916 supply with 19.6k/57.6k divider

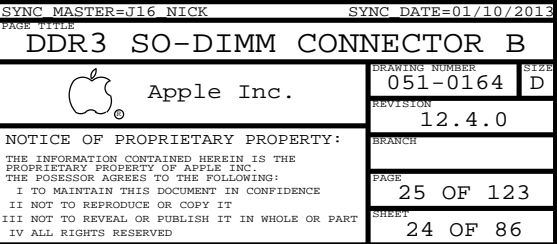
VRef Dividers

Always used, regardless of margining option.




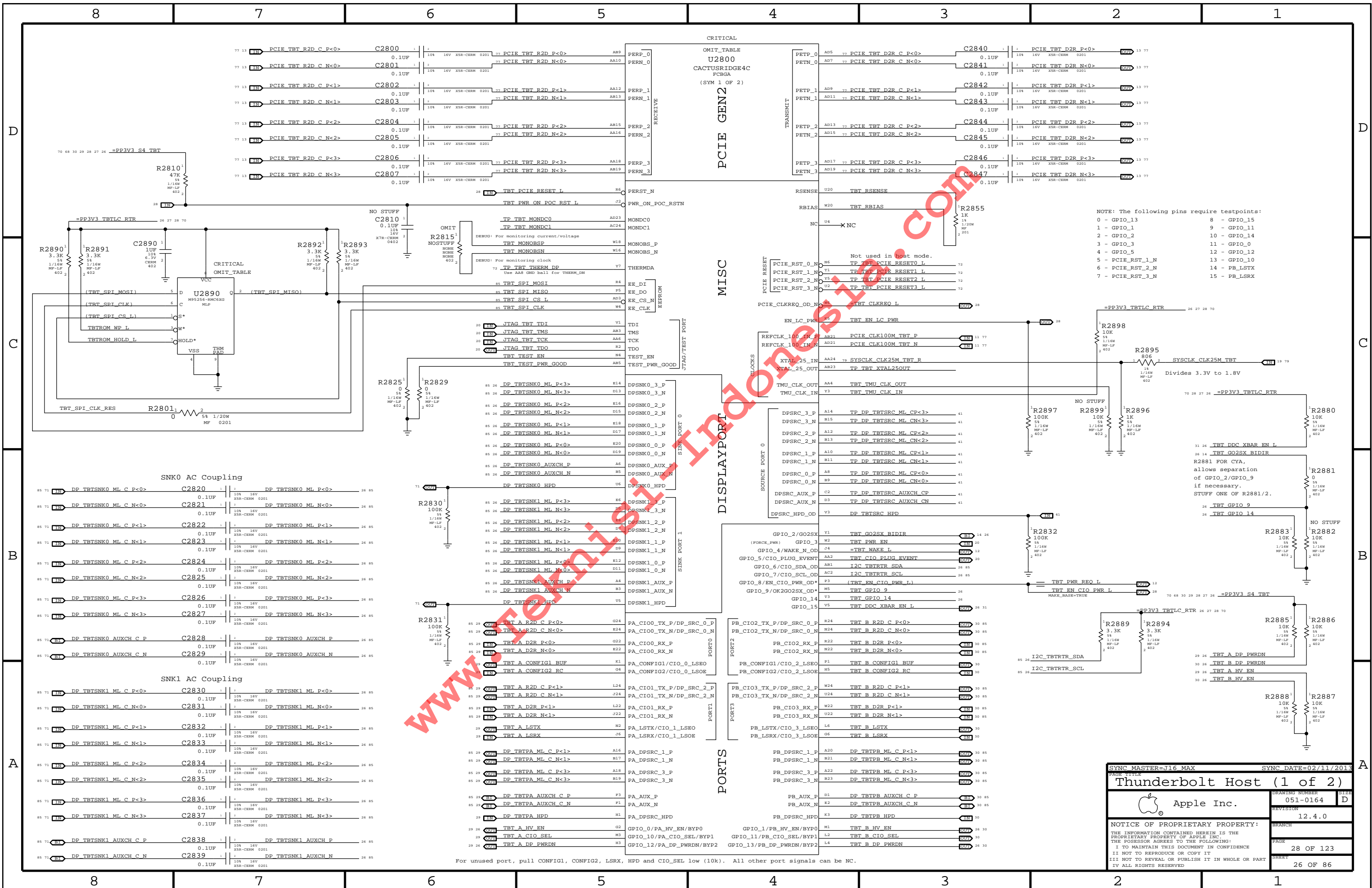
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PAGE TITLE		DDR3 VREF MARGINING	
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		REVISION	12.4.0
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8		7		6		5		4		3		2		1	
THERE ARE NO PIN SWAPS															
D	75	MEM A DQS N<0>	==	=MEM A DQS N<0>	23	75	MEM B DQS N<0>	==	=MEM B DQS N<0>	24					
	75	MEM A DQS P<0>	==	=MEM A DQS P<0>	23	75	MEM B DQS P<0>	==	=MEM B DQS P<0>	24					
	75	MEM A DQ<7>	==	=MEM A DQ<7>	23	75	MEM B DQ<7>	==	=MEM B DQ<7>	24					
	75	MEM A DQ<6>	==	=MEM A DQ<6>	23	75	MEM B DQ<6>	==	=MEM B DQ<6>	24					
	75	MEM A DQ<5>	==	=MEM A DQ<5>	23	75	MEM B DQ<5>	==	=MEM B DQ<5>	24					
	75	MEM A DQ<4>	==	=MEM A DQ<4>	23	75	MEM B DQ<4>	==	=MEM B DQ<4>	24					
	75	MEM A DQ<3>	==	=MEM A DQ<3>	23	75	MEM B DQ<3>	==	=MEM B DQ<3>	24					
	75	MEM A DQ<2>	==	=MEM A DQ<2>	23	75	MEM B DQ<2>	==	=MEM B DQ<2>	24					
	75	MEM A DQ<1>	==	=MEM A DQ<1>	23	75	MEM B DQ<1>	==	=MEM B DQ<1>	24					
	75	MEM A DQ<0>	==	=MEM A DQ<0>	23	75	MEM B DQ<0>	==	=MEM B DQ<0>	24					
C	75	MEM A DQS N<1>	==	=MEM A DQS N<1>	23	75	MEM B DQS N<1>	==	=MEM B DQS N<1>	24					
	75	MEM A DQS P<1>	==	=MEM A DQS P<1>	23	75	MEM B DQS P<1>	==	=MEM B DQS P<1>	24					
	75	MEM A DQ<15>	==	=MEM A DQ<15>	23	75	MEM B DQ<15>	==	=MEM B DQ<15>	24					
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	75	MEM A DQ<13>	==	=MEM A DQ<13>	23	75	MEM B DQ<13>	==	=MEM B DQ<13>	24					
	75	MEM A DQ<12>	==	=MEM A DQ<12>	23	75	MEM B DQ<12>	==	=MEM B DQ<12>	24					
	75	MEM A DQ<11>	==	=MEM A DQ<11>	23	75	MEM B DQ<11>	==	=MEM B DQ<11>	24					
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	75	MEM A DQ<8>	==	=MEM A DQ<8>	23	75	MEM B DQ<8>	==	=MEM B DQ<8>	24					
B	75	MEM A DQS N<2>	==	=MEM A DQS N<2>	23	75	MEM B DQS N<2>	==	=MEM B DQS N<2>	24					
	75	MEM A DQS P<2>	==	=MEM A DQS P<2>	23	75	MEM B DQS P<2>	==	=MEM B DQS P<2>	24					
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A	75	MEM A DQS N<3>	==	=MEM A DQS N<3>	23	75	MEM B DQS N<3>	==	=MEM B DQS N<3>	24					
	75	MEM A DQS P<3>	==	=MEM A DQS P<3>	23	75	MEM B DQS P<3>	==	=MEM B DQS P<3>	24					
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	75	MEM A DQ<27>	==	=MEM A DQ<27>	23	75	MEM B DQ<27>	==	=MEM B DQ<27>	24					
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SYNC_MASTER=J16_NICK SYNC_DATE=01/10/2013															
DDR3 ALIASES AND BITSWAPS															
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DDR3 ALIASES AND BITSWAPS			
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PAGE TITLE			
Thunderbolt Host		(1 of 2)	
	Apple Inc.	DRAWING NUMBER	051-0164
		SIZE	D
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Page Notes

Power aliases required by this page:

- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTWRCCTL
- =PP1V05_TBT_P1V05TBTFFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

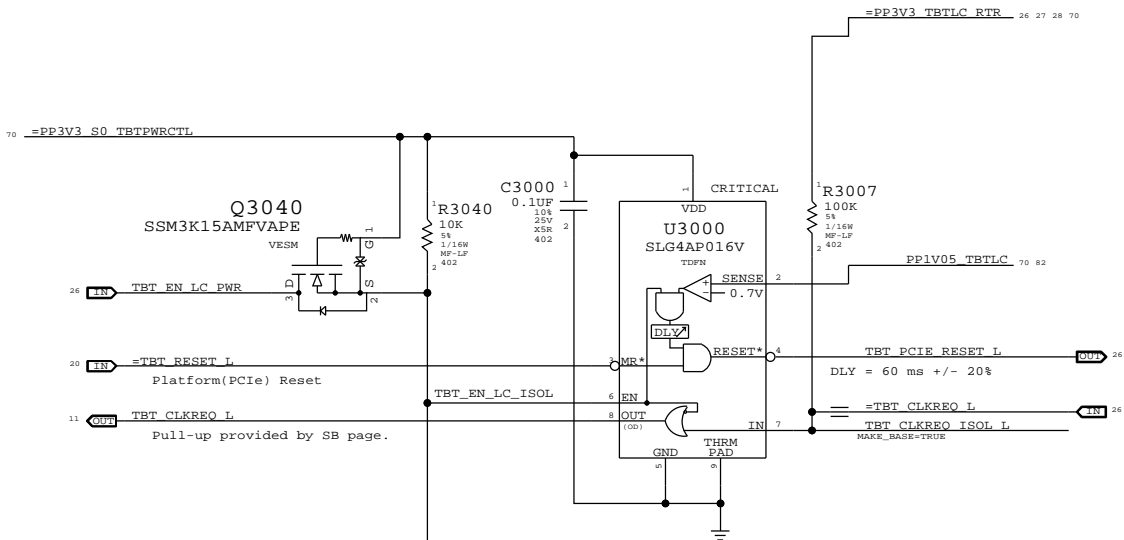
Signal aliases required by this page:

- =TBT_CLKREQ_L
- =TBT_RESET_L

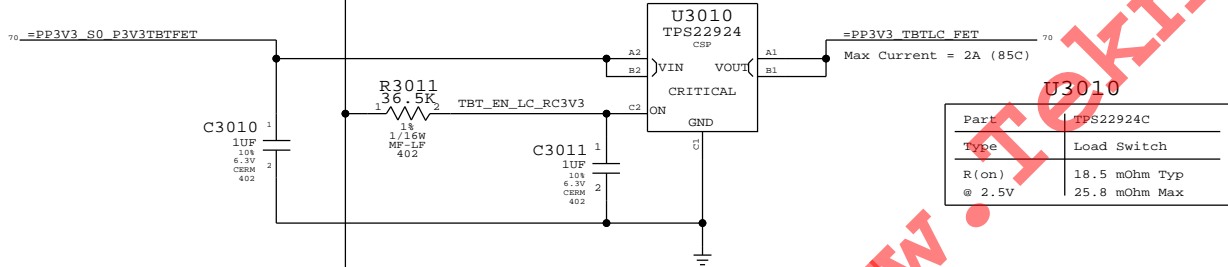
BOM options provided by this page:

TBTBST:Y - Stuffs 15V boost circuitry.

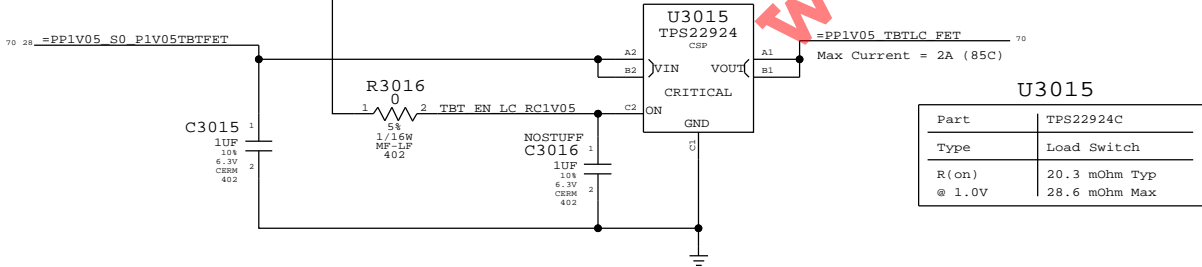
Supervisor & CLKREQ# Isolation



3.3V TBT "LC" Switch

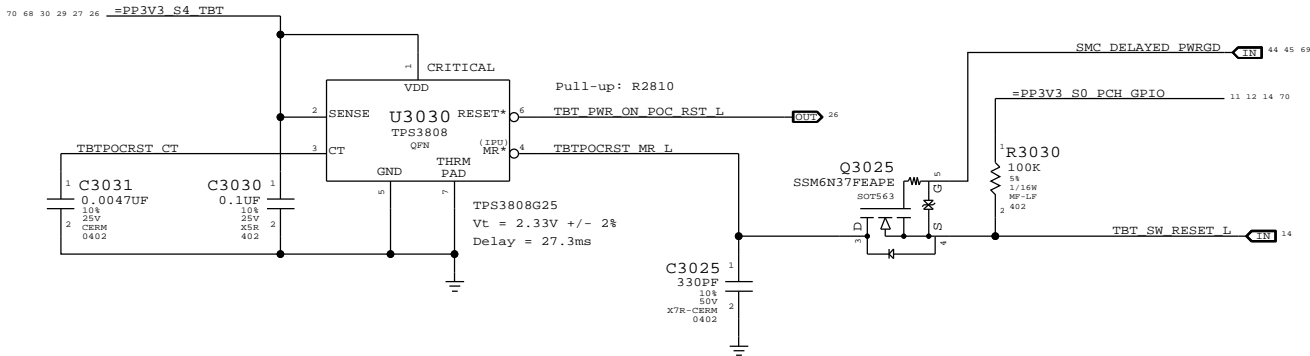


1.05V TBT "LC" Switch

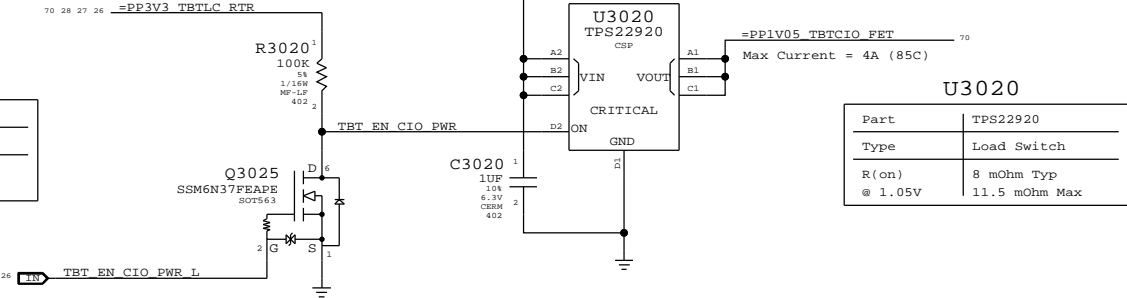


TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.



1.05V TBT "CIO" Switch



SYNC MASTER=J16 MAX SYNC DATE=02/11/2013

Thunderbolt Power Support

Apple Inc.

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D

B


```
DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low:  0 - 0.8V
```



C



SYNCH MASTER=J16 MAX		SYNCH DATE=02/11/2013	
PAGE TITLE			
Thunderbolt Connector A			
 Apple Inc.		DRAWING NUMBER 051-0164	SIZE D
		REVISION 12.4.0	
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8	7	6	5	4	3	2	1
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D



B



8	7	6	5	4	3	2	1
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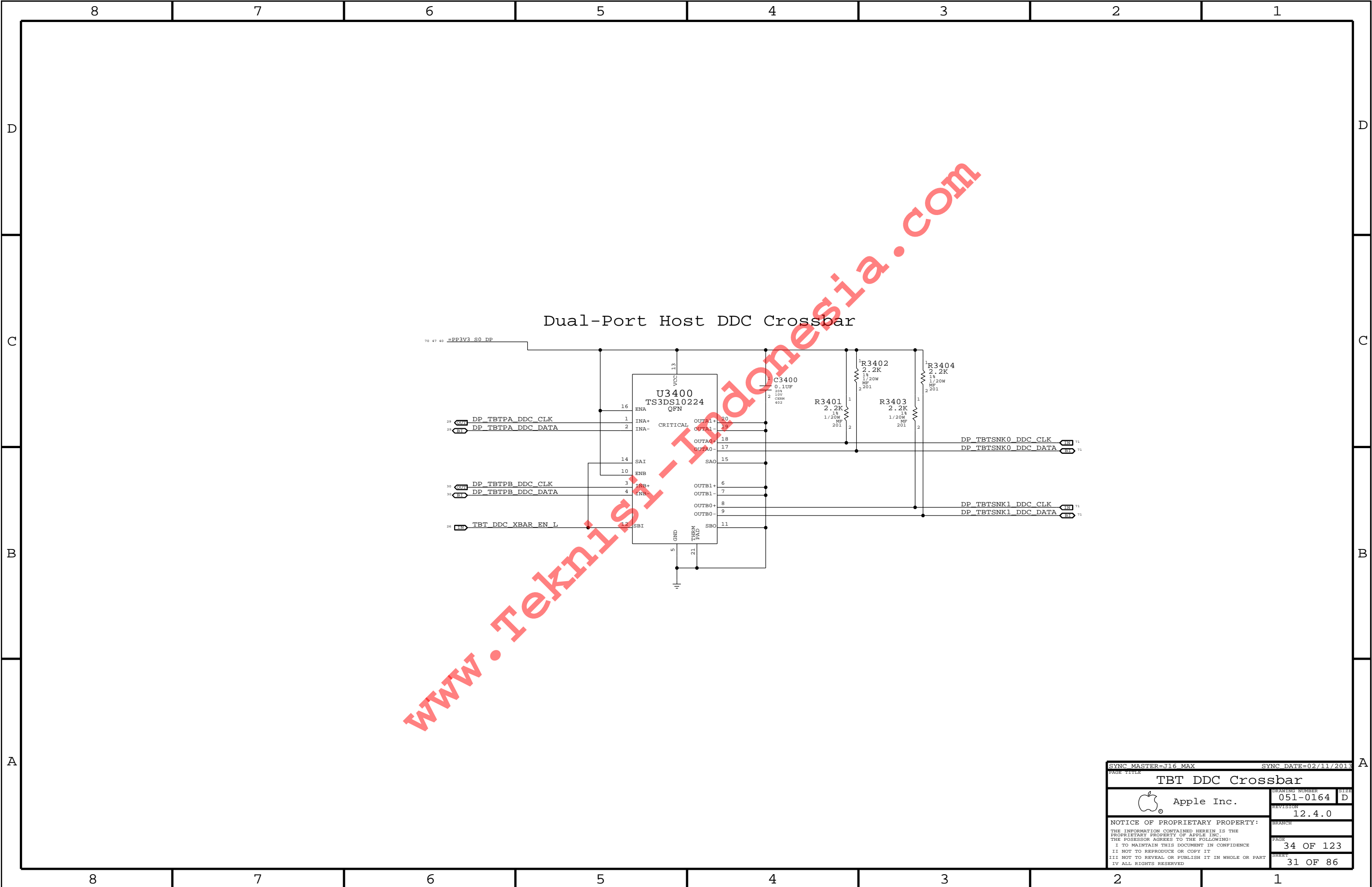


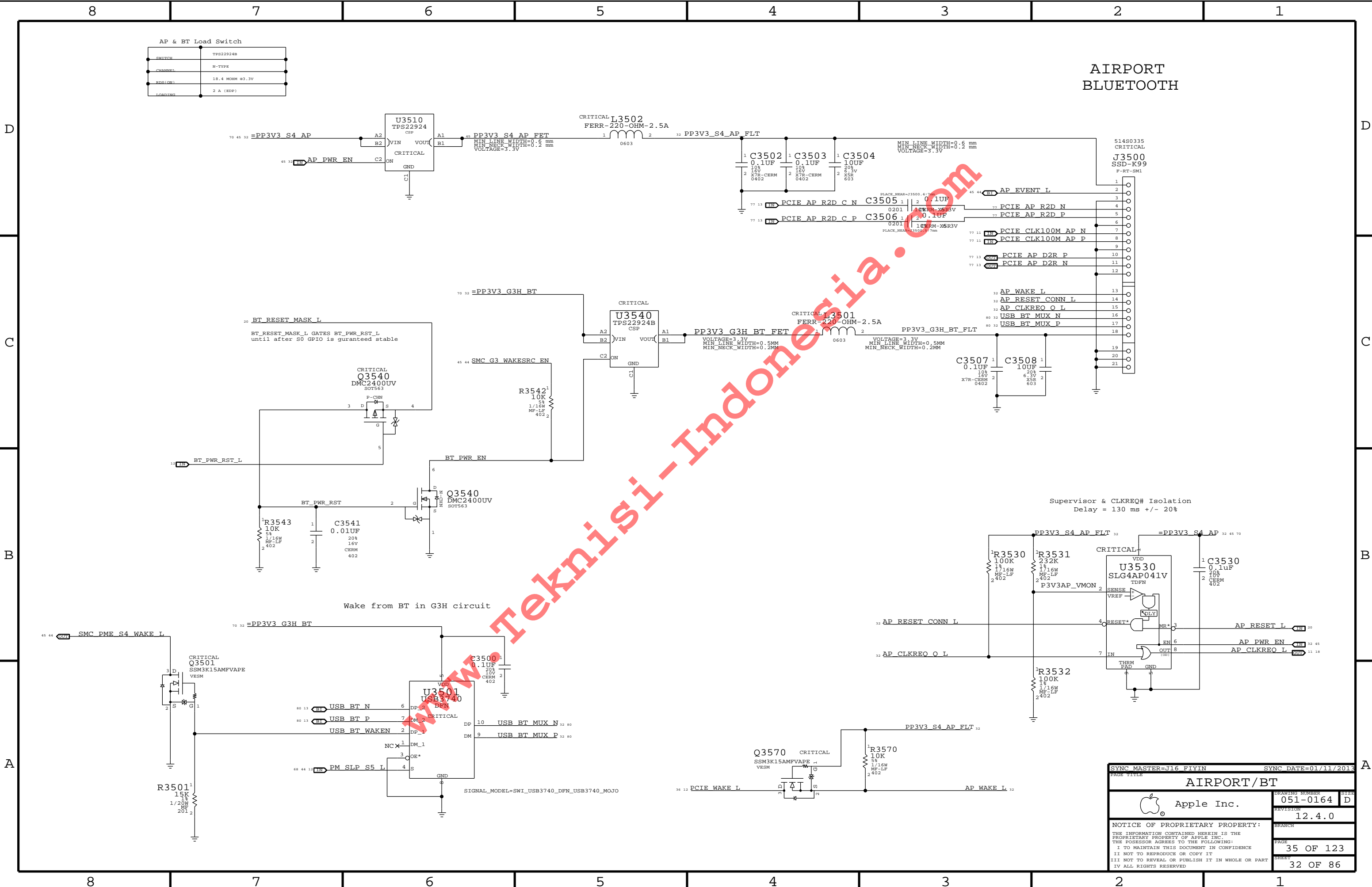
C



A

A

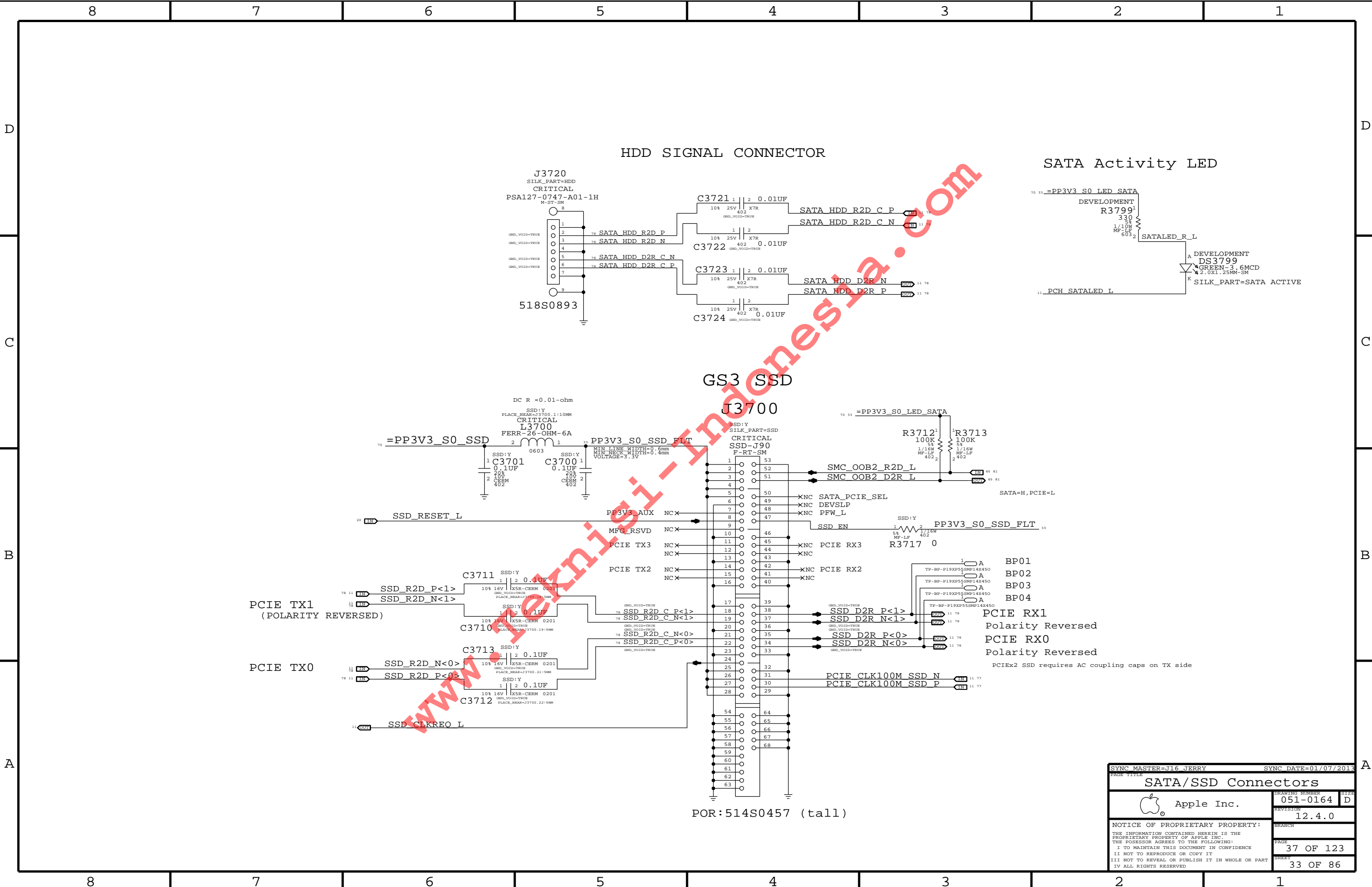





AP & BT Load Switch	
SWITCH	TPS22924B
CHANNEL	N-TYPE
RES(ON)	18.4 MOHM @3.3V
LOADING	2 A (BDP)

AIRPORT
BLUE TOOTH

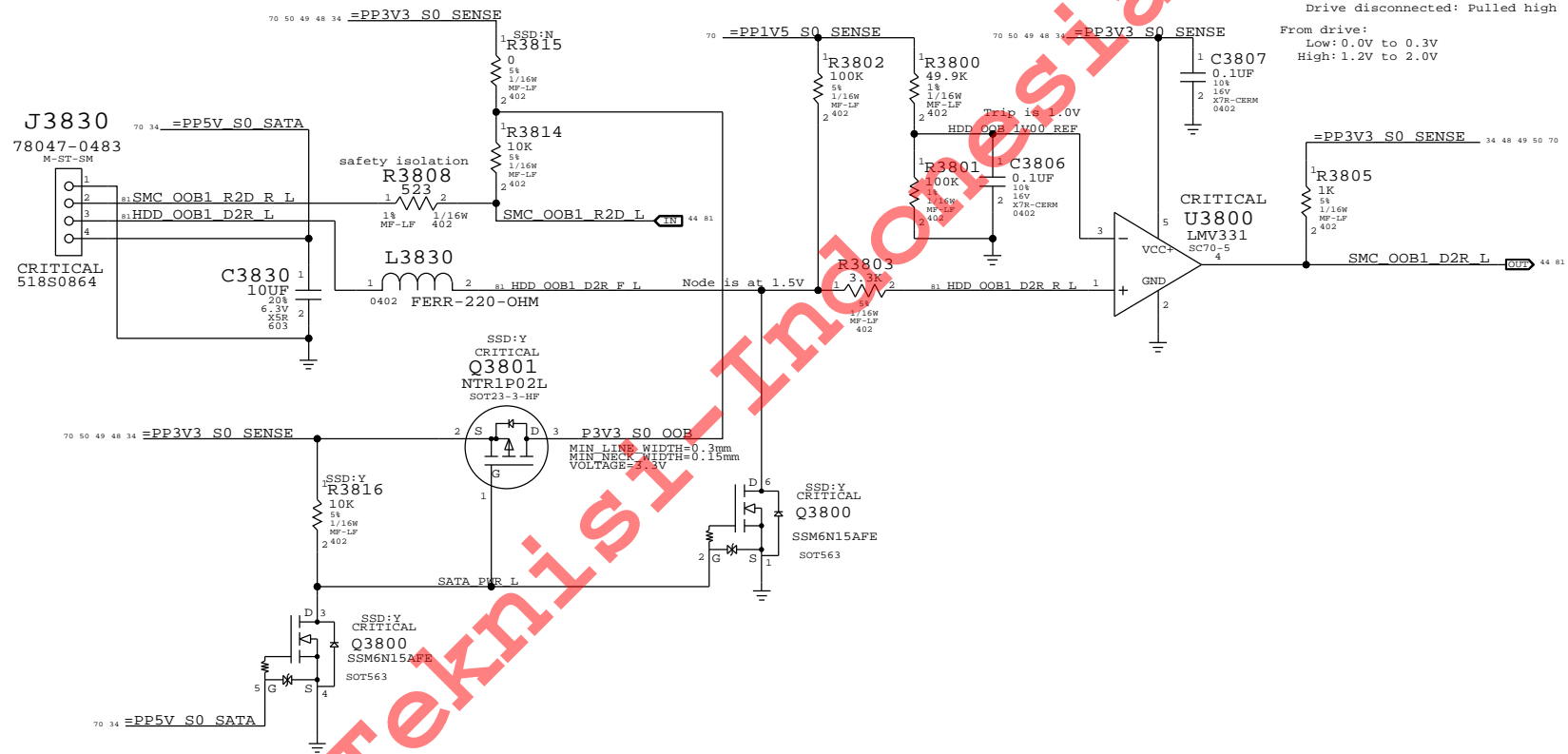
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AIRPORT/BT		DRAWING NUMBER	
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SATA/SSD Connectors			
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HDD POWER/OOB CONNECTOR

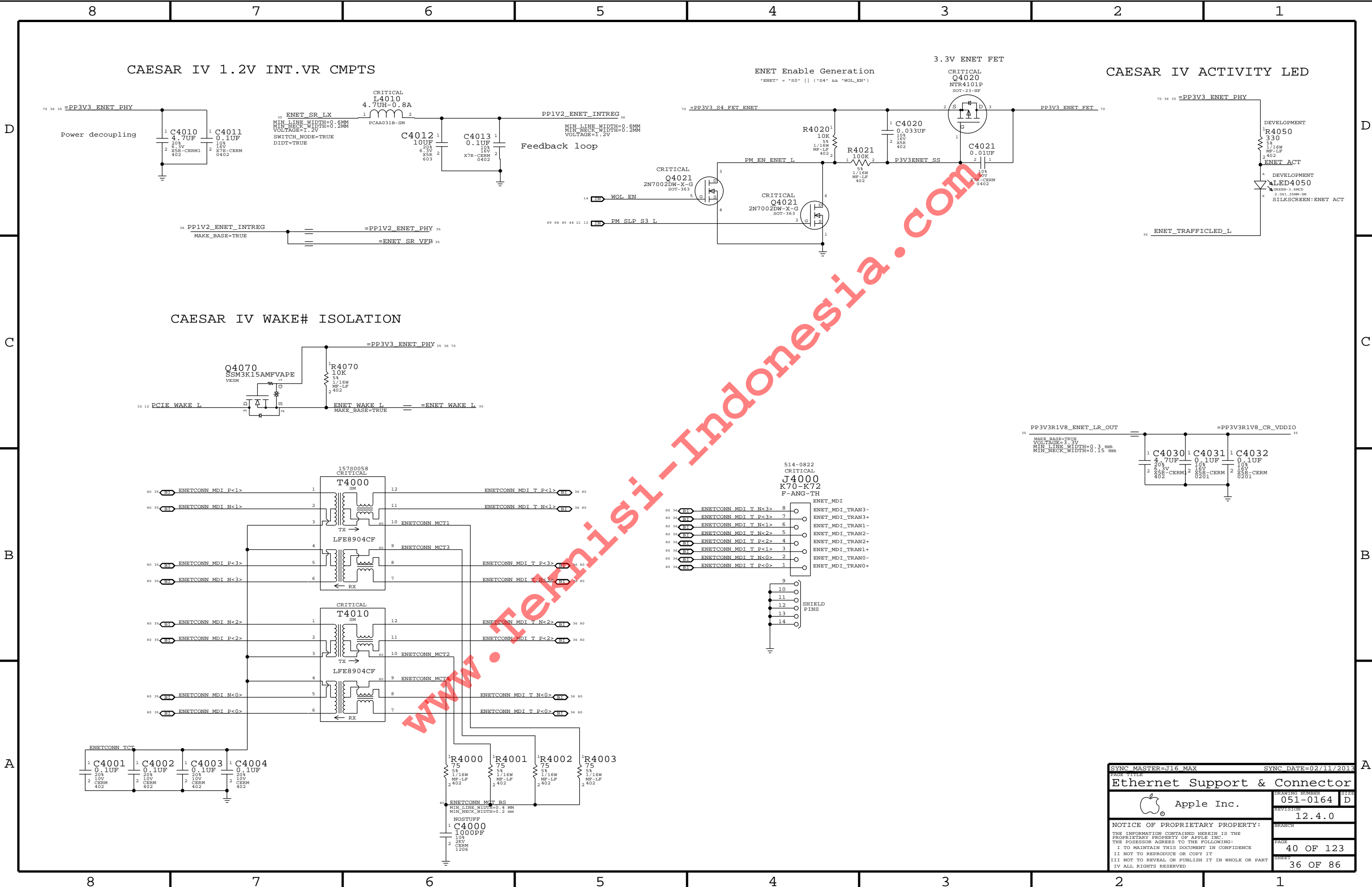
HDD Out-of-Band Temperature Sensing



Notes:
Drive active: Valid signal protocol
Drive asleep: HDD drives HDD_OOB_TEMP low
Drive disconnected: Pulled high

From drive:
Low: 0.0V to 0.3V
High: 1.2V to 2.0V

SYNC MASTER=J16 JERRY		SYNC DATE=01/07/2013	
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HDD Connector			
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353S2548

U4100
TPS2553
SON
CRITICAL

IN 6
EN 4
GND 5
THERML PAD 7
OUT 1
ILIM 2
SDCONN OC L 3
SDCONN ILIM R 12

70 PP3V3_S0_SDCARD
15 ENET_CR_PWR
PP3V3_S0_SW_SD_PWR
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4 mm
MIN_PAD_SIZE=0.2 mm
MOUNTAGE=3.3V

C4100 22UF 1 2
X5R-CERM1 0603
6.3V 204

C4101 0.1UF 1 2
X7R-CERM 0402
10V 194

C4102 10UF 1 2
X5R-CERM 603
6.3V 204

C4103 0.1UF 1 2
X5R-CERM 0402
16V 194

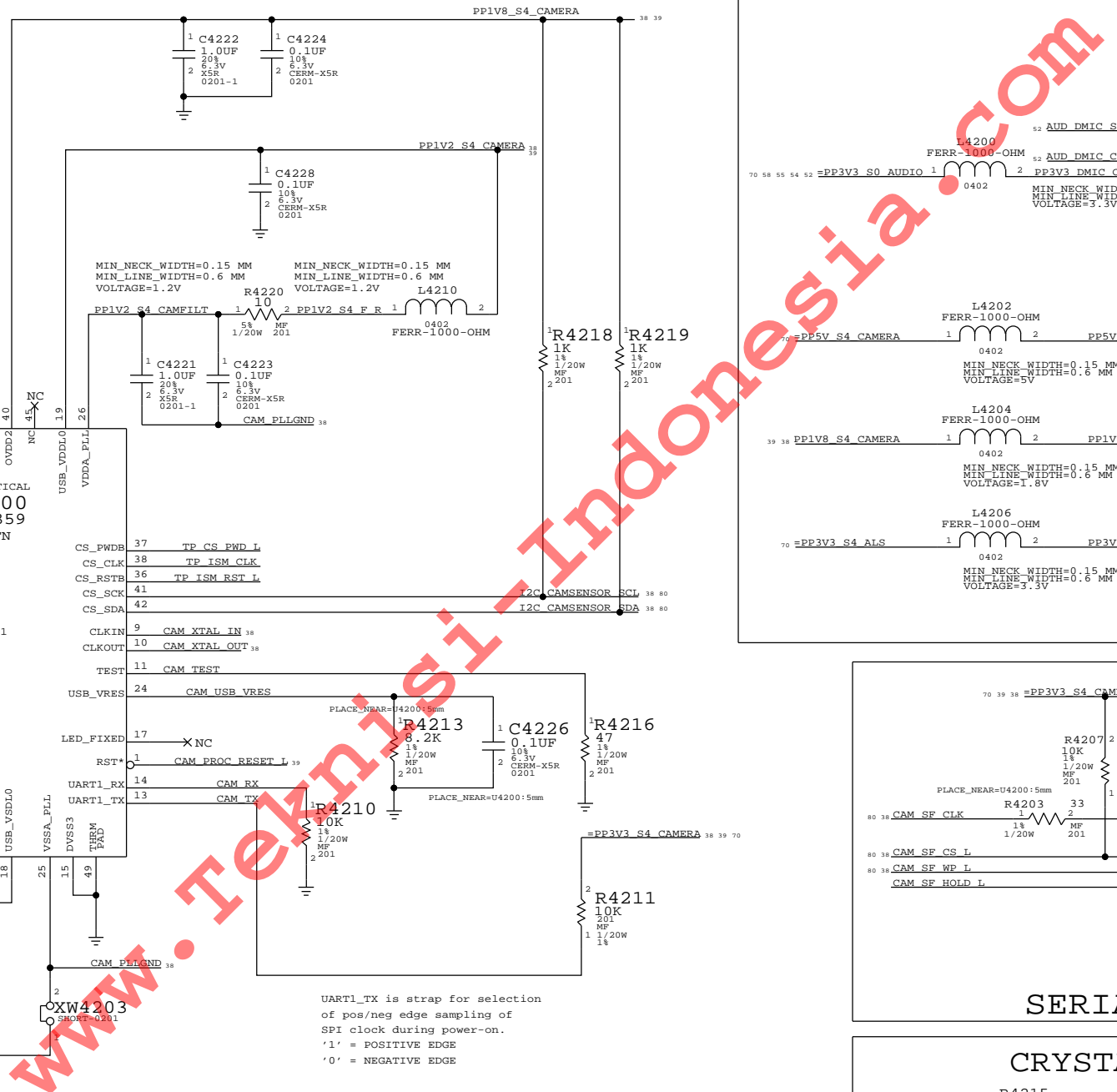
R4118 13K 1 2
1/16W 0402
10K 194

R4119 13K 1 2
1/16W 0402
10K 194

R4100 47K 1 2
1/16W 0402
10K 194

[illegible][illegible]

A




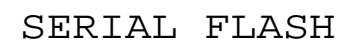
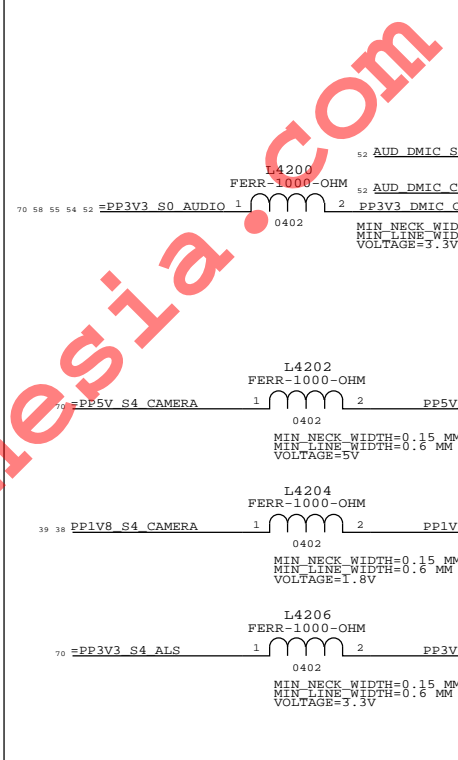
J4200
20455-A20E-32
F-RT-SM

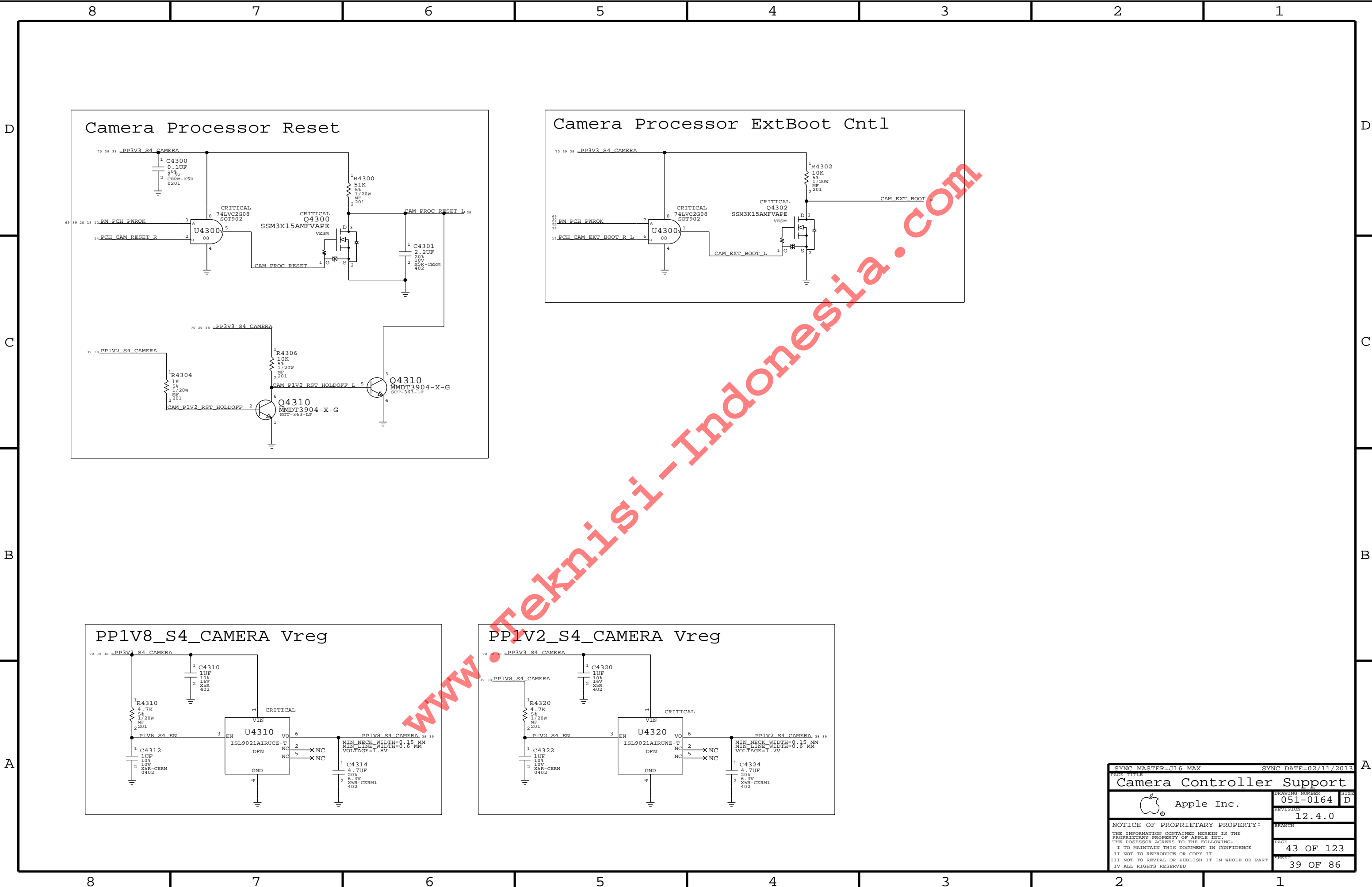
21 22 25

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

23 24 26

Ground





D

C

B

A

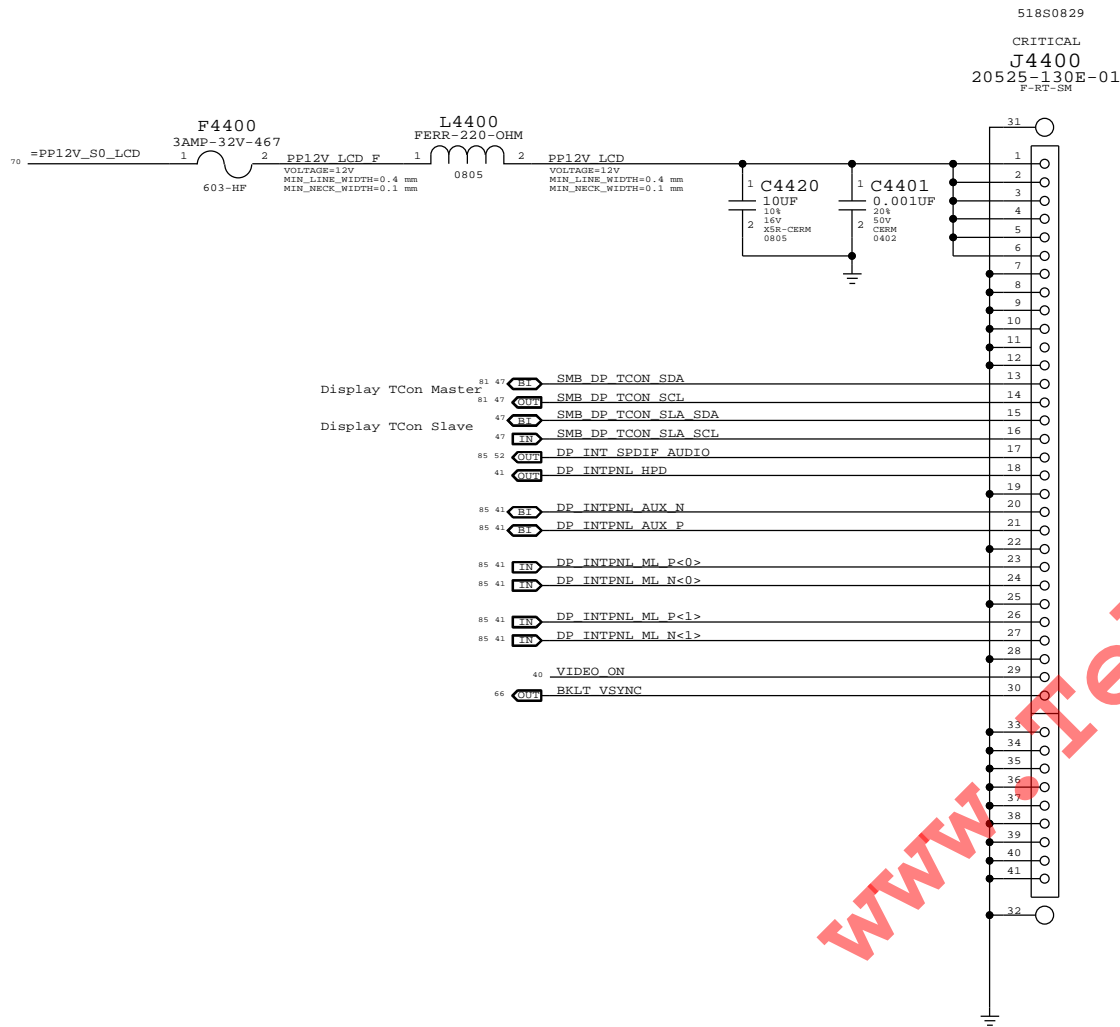
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C

B

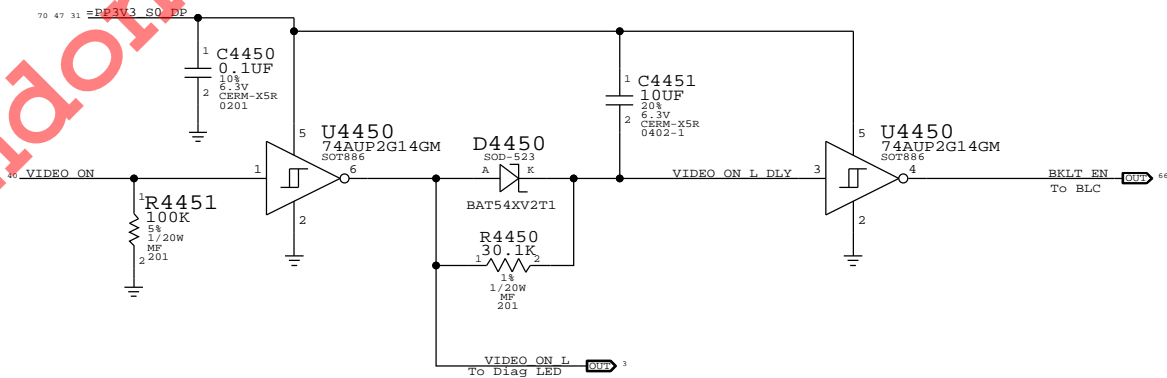
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
Internal DP Connector



Backlight Control

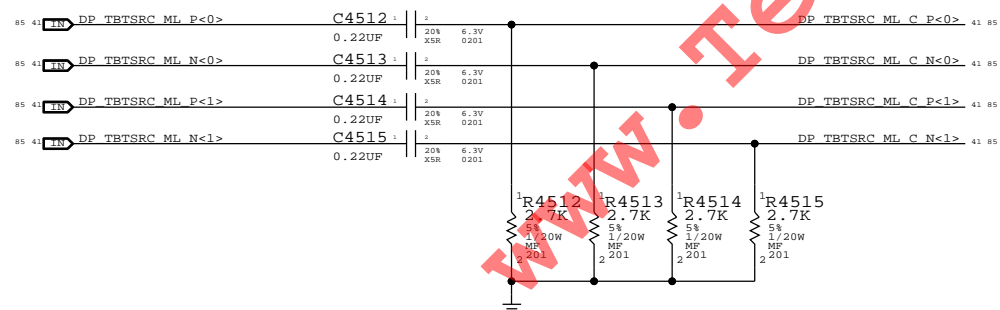
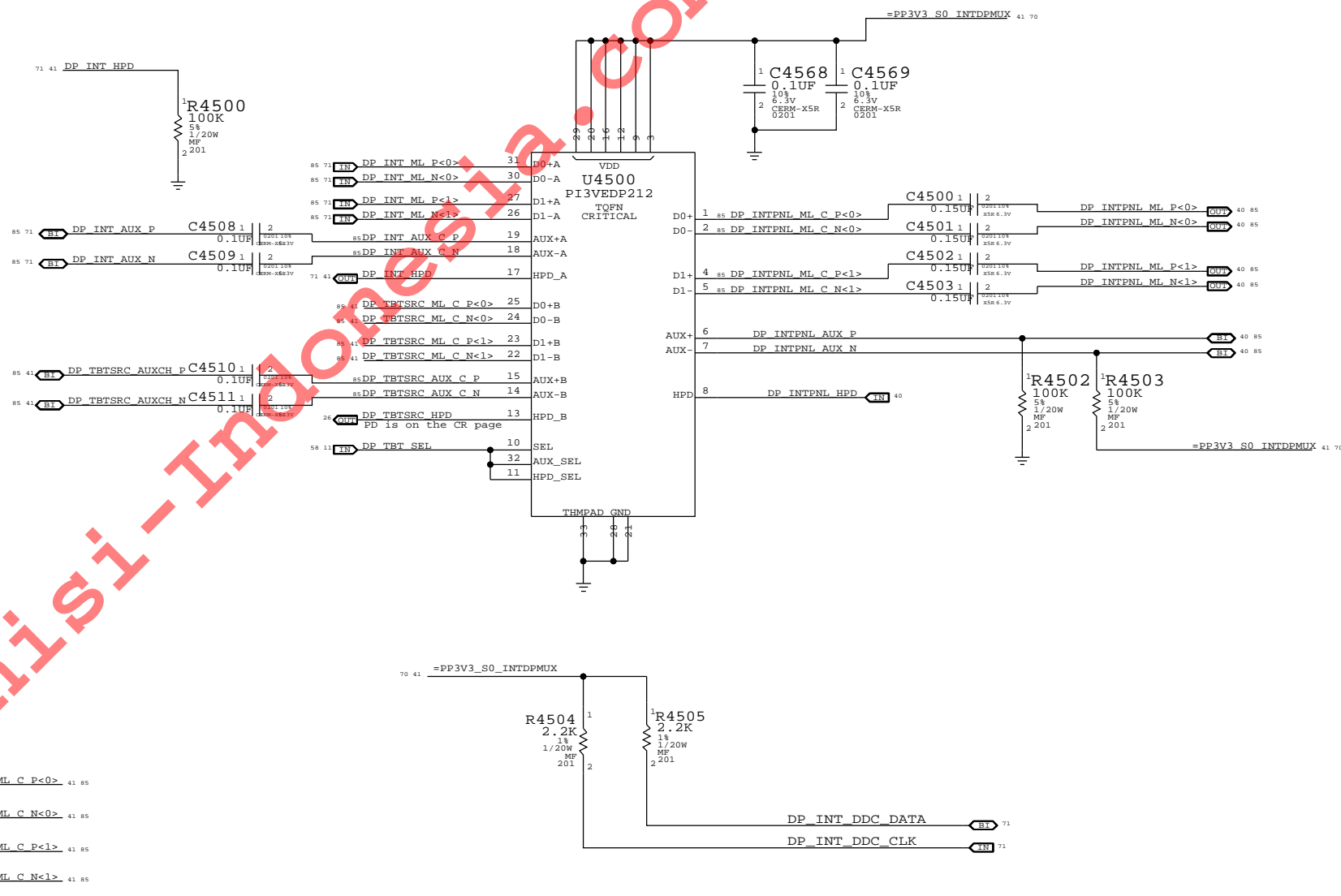
Delay applies only on a L->H transition on VIDEO_ON. This guarantees video is valid before the backlight is enabled.
On a H->L transition, output follows with standard logic propagation delay. This ensures the backlight is off immediately after loss of video

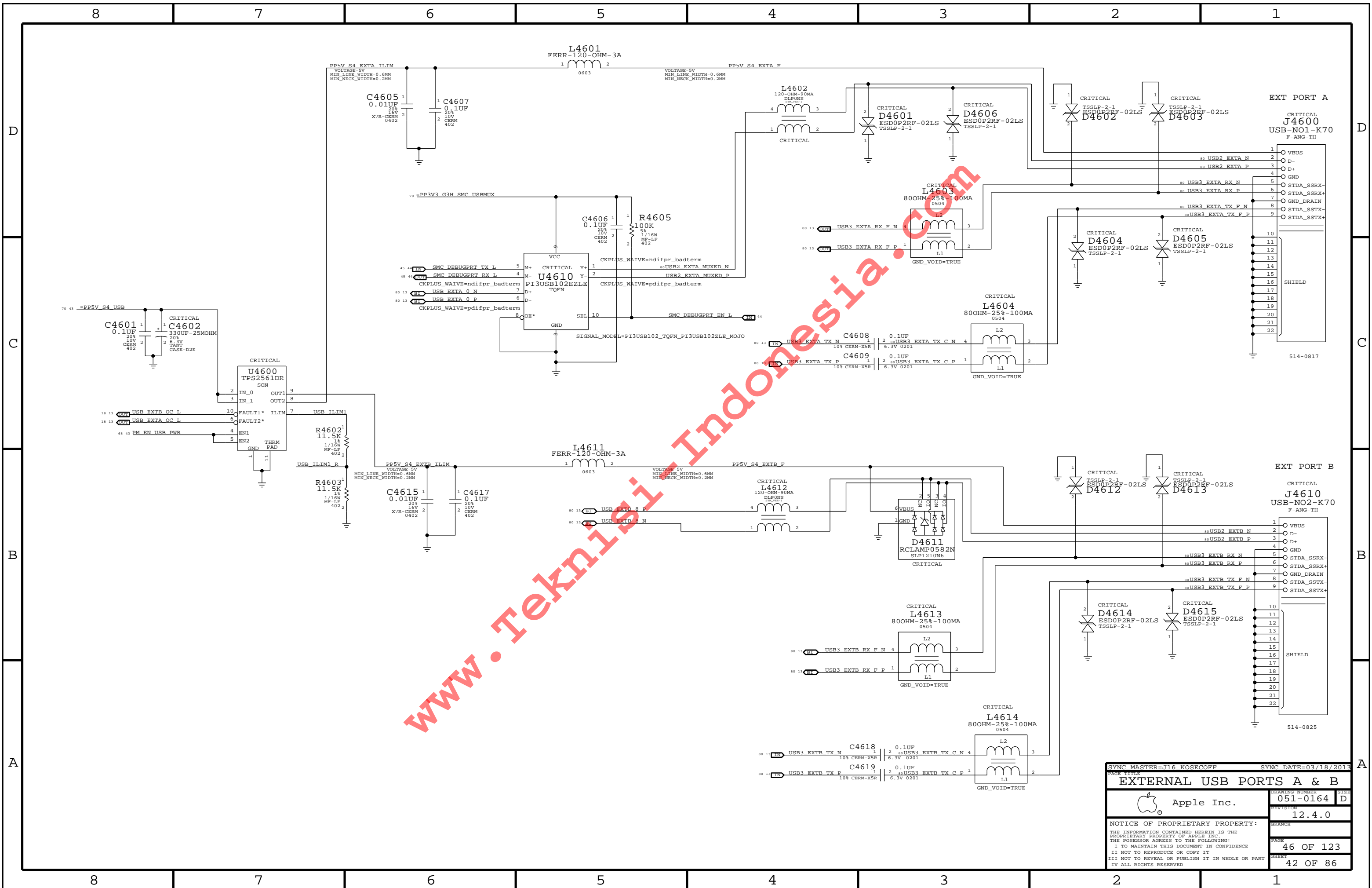


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Internal DP Support			
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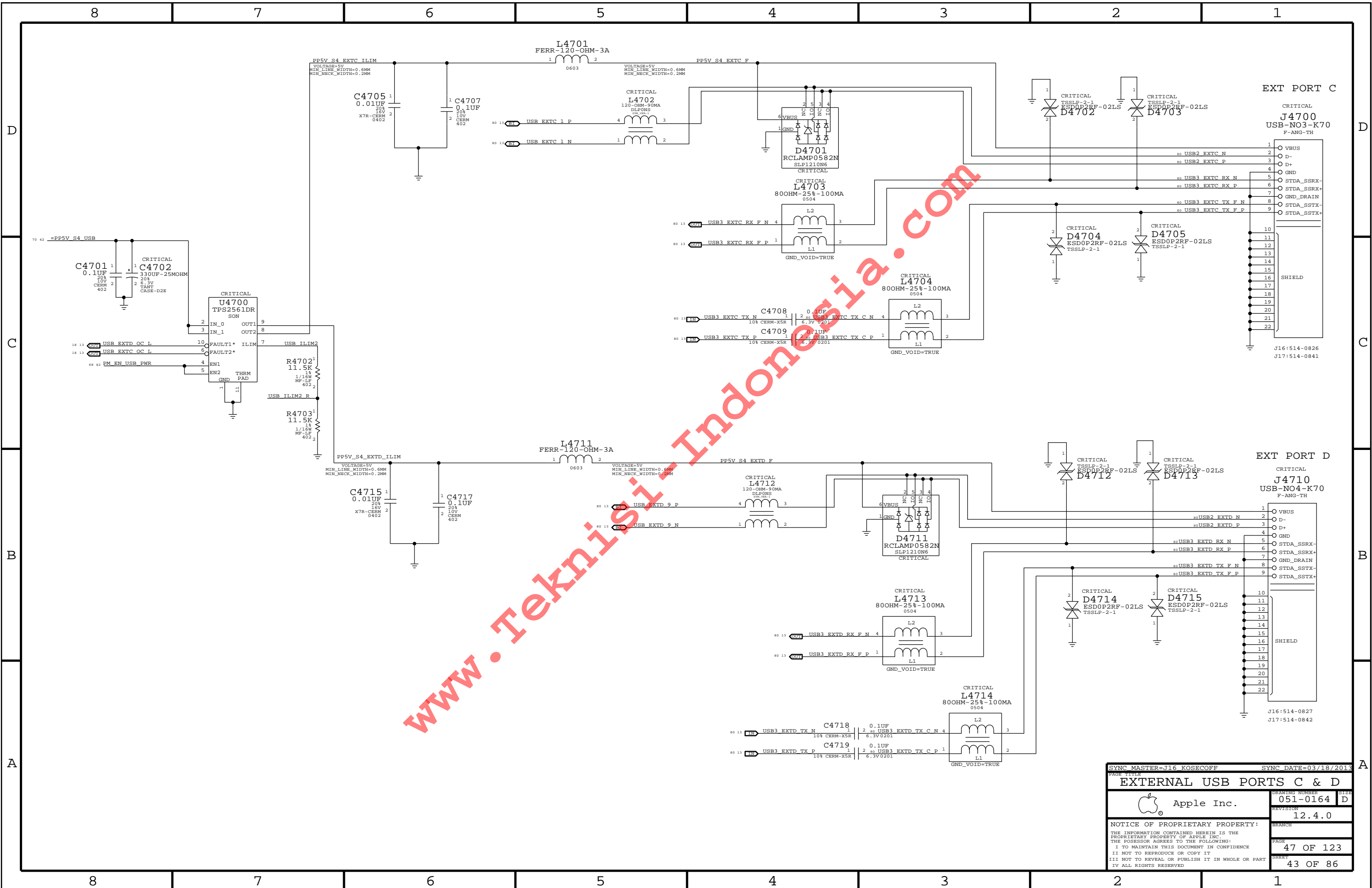
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					BASE_BASE=TRUE NAME_NAME=TRUE	
26		TP DP TBTSRC ML CN<0>	==		DP TBTSRC ML N<0>	41 89
					BASE_BASE=TRUE NAME_NAME=TRUE	
26		TP DP TBTSRC ML CP<1>	==		DP TBTSRC ML P<1>	41 89
					BASE_BASE=TRUE NAME_NAME=TRUE	
26		TP DP TBTSRC ML CN<1>	==		DP TBTSRC ML N<1>	41 89
					BASE_BASE=TRUE NAME_NAME=TRUE	
26		TP DP TBTSRC AUXCH CP	==		DP TBTSRC AUXCH P	41 89
					BASE_BASE=TRUE NAME_NAME=TRUE	
26		TP DP TBTSRC AUXCH CN	==		DP TBTSRC AUXCH N	41 89
					BASE_BASE=TRUE NAME_NAME=TRUE	


24	TP	DP	TBTSRC	ML	CP<2>	=	NC	DP	TBTSRC	ML	P<2>	
											NO_TEST-TRUE	MAKE_BASE-TRUE
26	TP	DP	TBTSRC	ML	CN<2>	=	NC	DP	TBTSRC	ML	N<2>	
											NO_TEST-TRUE	MAKE_BASE-TRUE
28	TP	DP	TBTSRC	ML	CP<3>	=	NC	DP	TBTSRC	ML	P<3>	
											NO_TEST-TRUE	MAKE_BASE-TRUE
26	TP	DP	TBTSRC	ML	CN<3>	=	NC	DP	TBTSRC	ML	N<3>	
											NO_TEST-TRUE	MAKE_BASE-TRUE
75	DP	INT	ML	P<2>	=	NC	DP	INT	ML	P<2>		
											NO_TEST-TRUE	MAKE_BASE-TRUE
75	DP	INT	ML	N<2>	=	NC	DP	INT	ML	N<2>		
											NO_TEST-TRUE	MAKE_BASE-TRUE
75	DP	INT	ML	P<3>	=	NC	DP	INT	ML	P<3>		
											NO_TEST-TRUE	MAKE_BASE-TRUE
75	DP	INT	ML	N<3>	=	NC	DP	INT	ML	N<3>		
											NO_TEST-TRUE	MAKE_BASE-TRUE

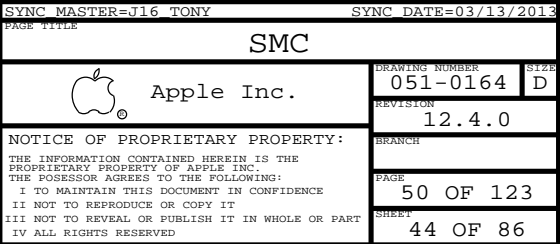


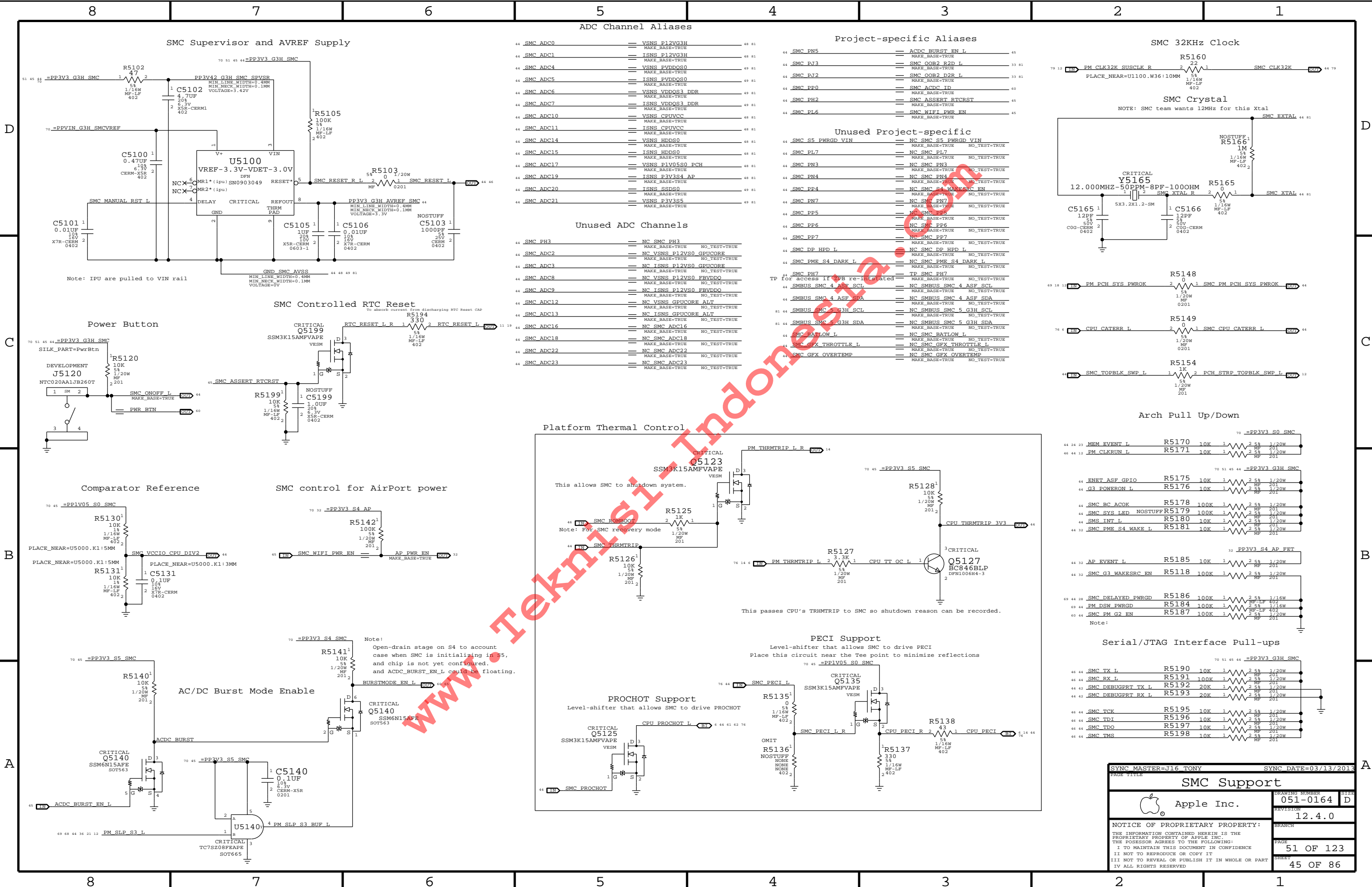


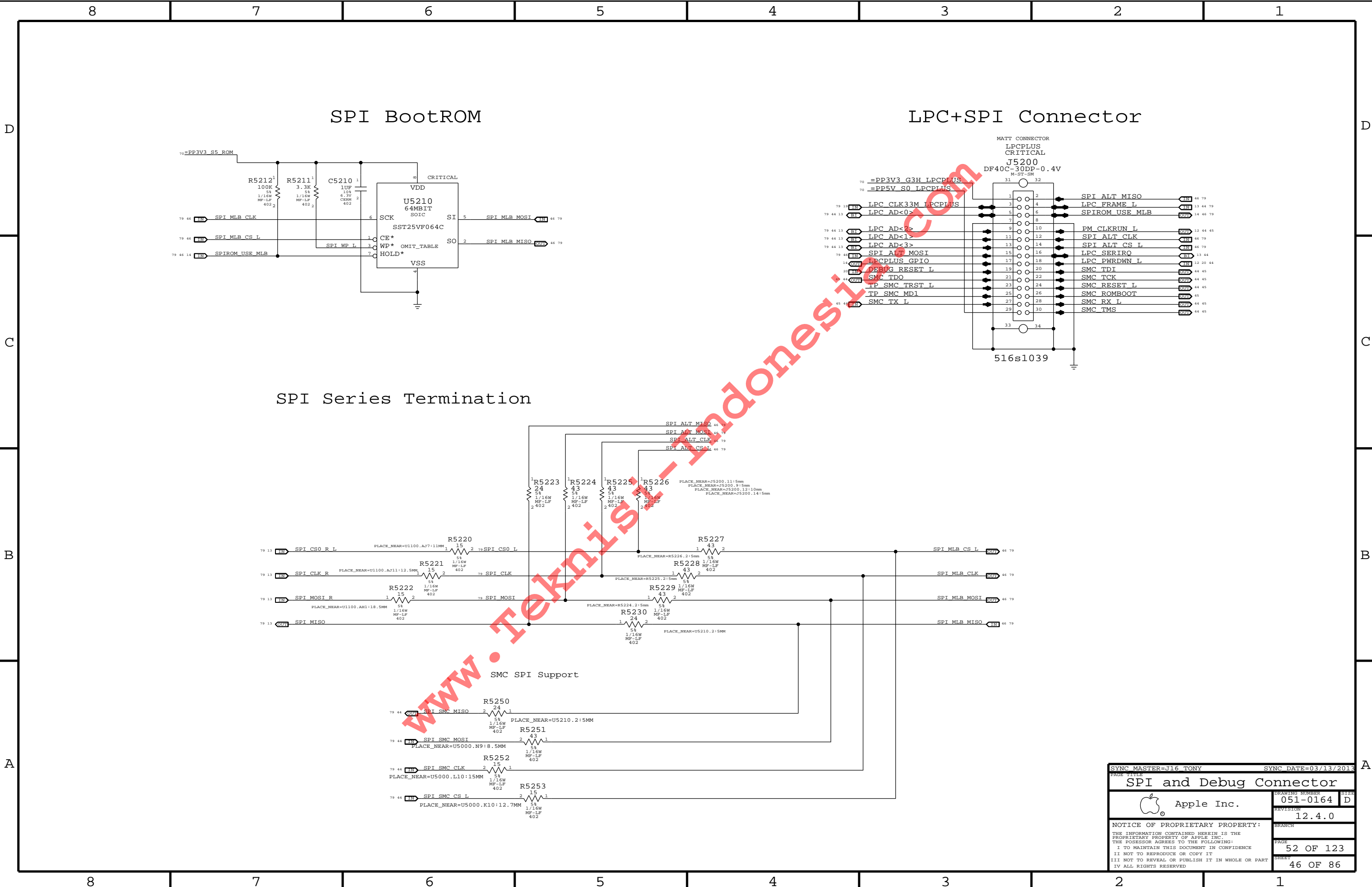
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PAGE TITLE		EXTERNAL USB PORTS A & B	
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


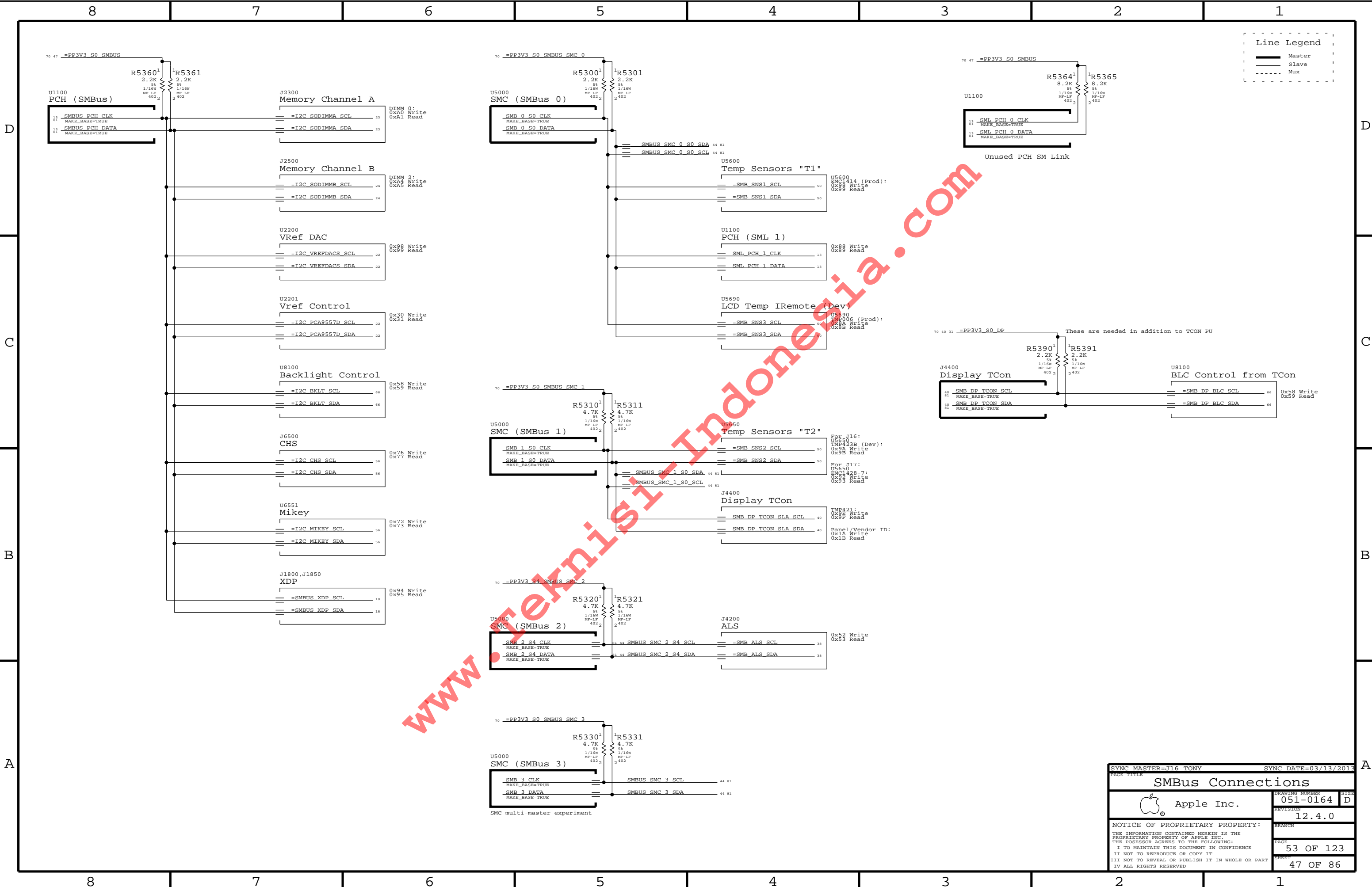
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EXTERNAL USB PORTS C & D			
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		REVISION	12.4.0
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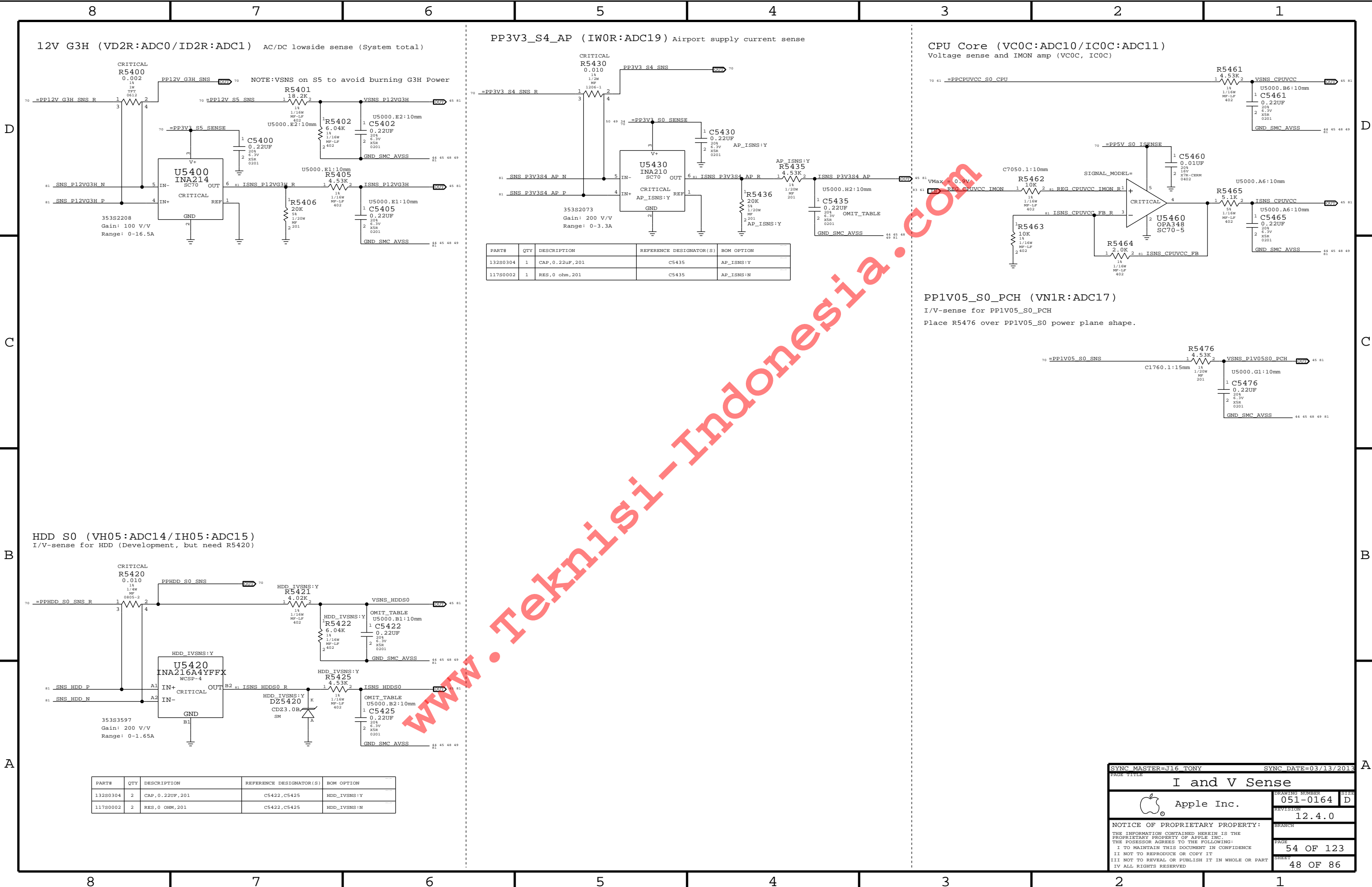




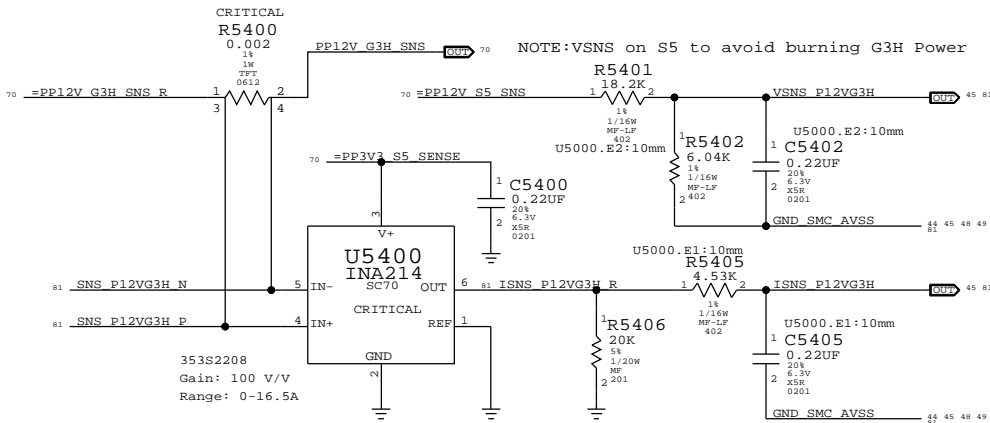


SYNC MASTER=J16 TONY		SYNC DATE=03/13/2013	
PAGE TITLE			
SPI and Debug Connector			
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		REVISION	12.4.0
		BRANCH	
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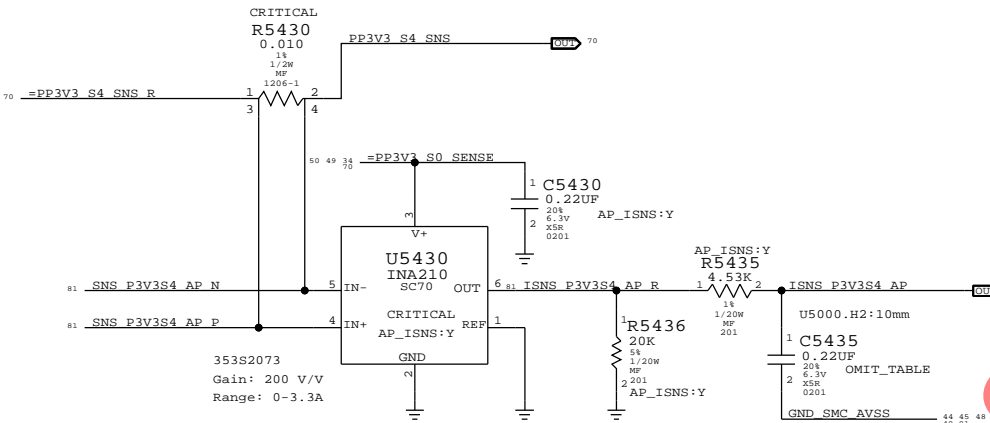




12V G3H (VD2R:ADC0/ID2R:ADC1) AC/DC lowside sense (System total)

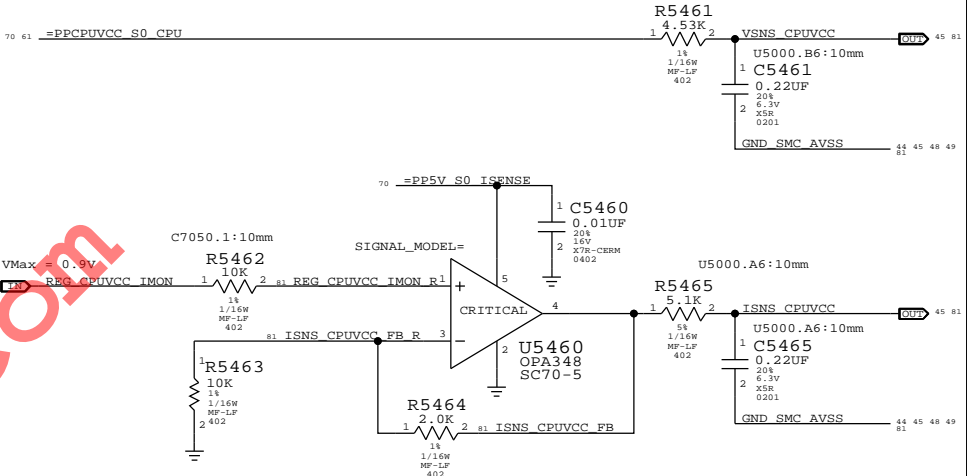


PP3V3_S4_AP (IW0R:ADC19) Airport supply current sense



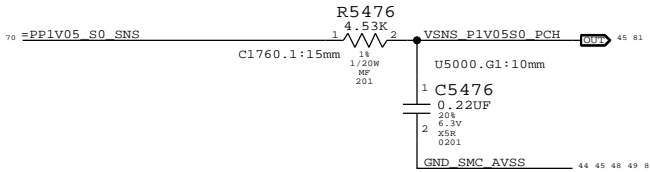
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	1	CAP,0.22uF,201	C5435	AP_ISNS:Y
117S0002	1	RES,0 ohm,201	C5435	AP_ISNS:N

CPU Core (VC0C:ADC10/IC0C:ADC11) Voltage sense and IMON amp (VC0C, IC0C)

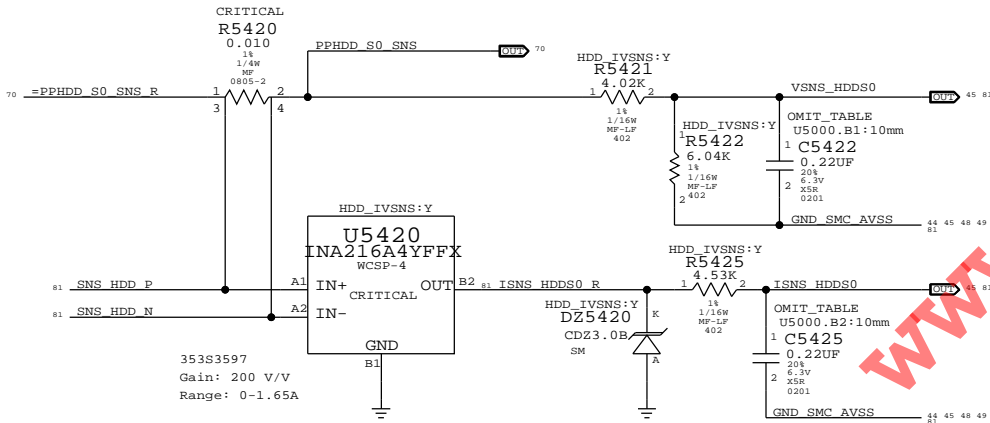


PP1V05_S0_PCH (VN1R:ADC17)

I/V-sense for PP1V05_S0_PCH
Place R5476 over PP1V05_S0 power plane shape.



HDD S0 (VH05:ADC14/IH05:ADC15) I/V-sense for HDD (Development, but need R5420)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	2	CAP,0.22uF,201	C5422,C5425	HDD_IVSNS:Y
117S0002	2	RES,0 OHM,201	C5422,C5425	HDD_IVSNS:N

SYNC MASTER=J16 TONY

SYNC DATE=03/13/2013

I and V Sense

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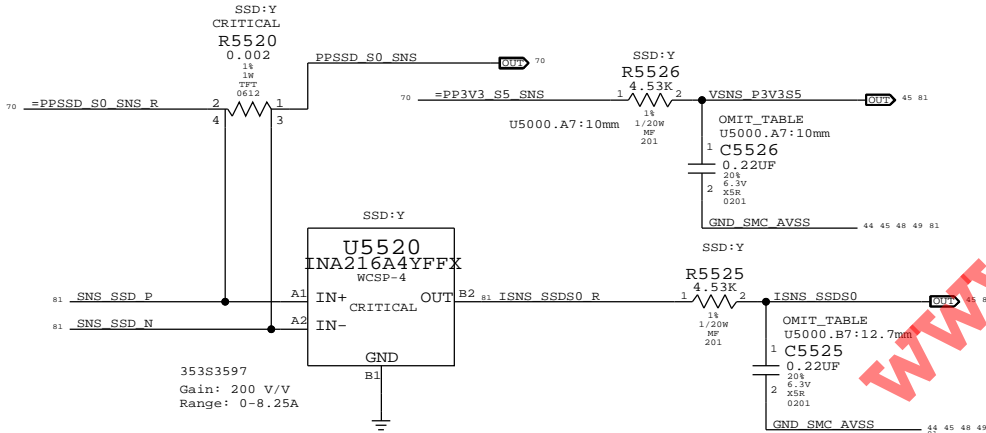
D

C

B

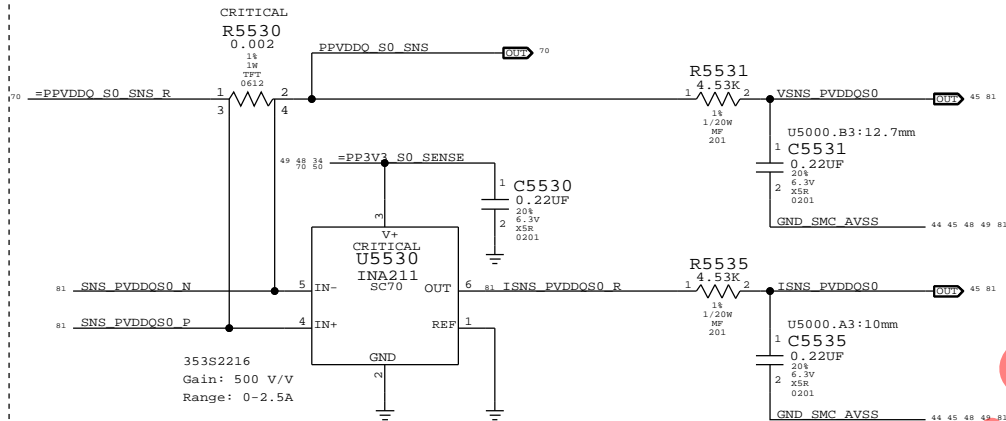
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SSD S0 (IH1R:ADC20/VR3R:ADC21) I-sense for SSD / V-sense for PP3V3_S5)

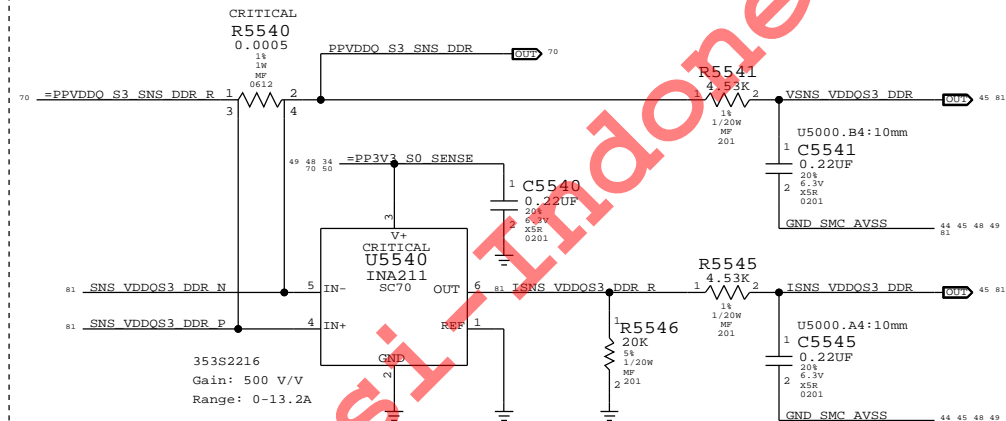


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	2	CAP,0.22UF,201	C5525,C5526	SSD:Y
117S0002	2	RES,0 OHM,201	C5525,C5526	SSD:N

PPVDDQ_S0 (VC0M:ADC4/IC0M:ADC5)
lowside sense for CPU mem rail (2.5A max draw, 3.3A max sense capability)



VDDQ S3 (VM0R:ADC6/IM0R:ADC7)
VDDQ lowside sense for SO-DIMM modules



SYNC MASTER=J16 TONY

SYNC DATE=03/13/2013

I and V Sense(Continued)

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051-0164

SIZE

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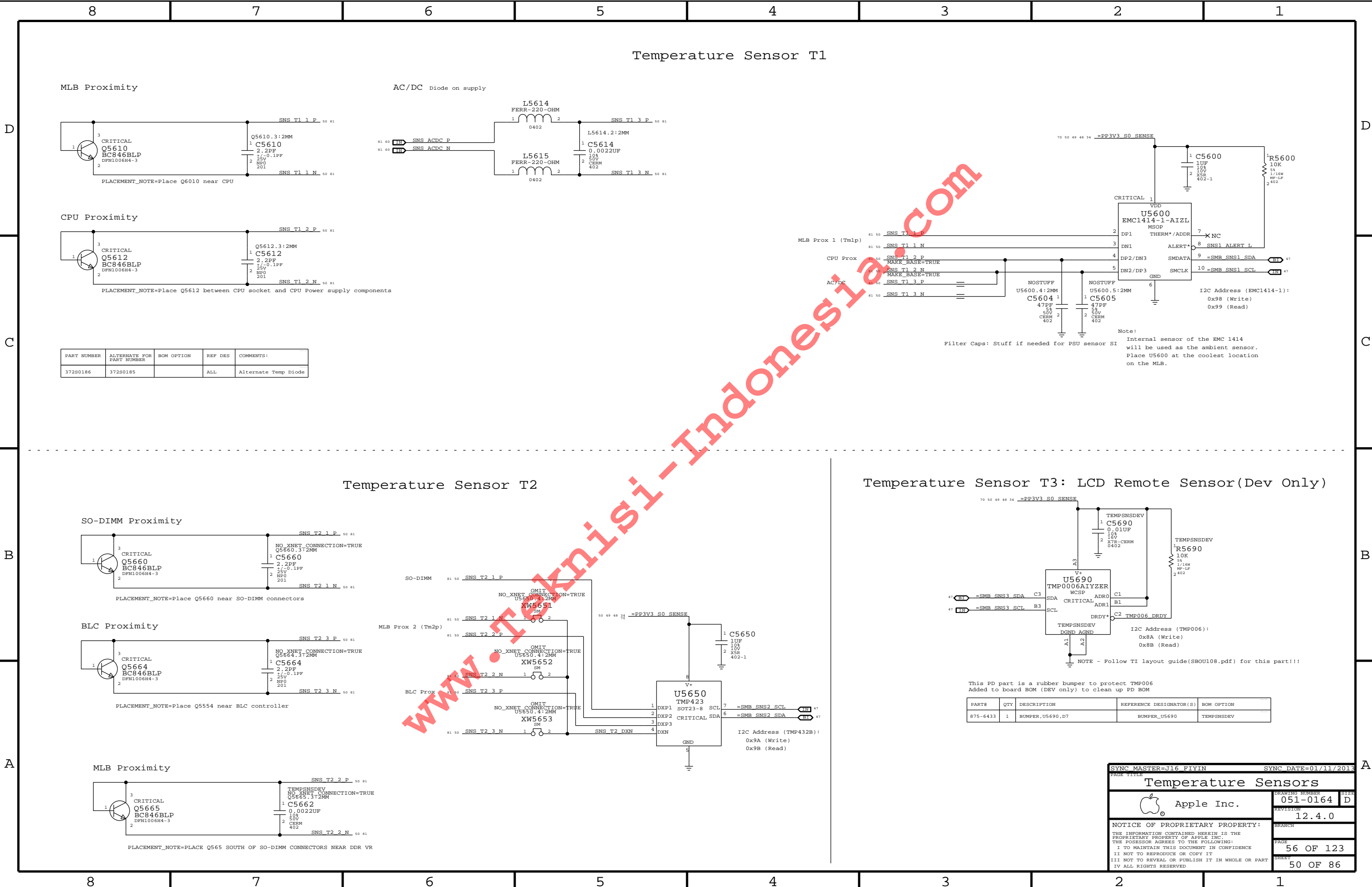
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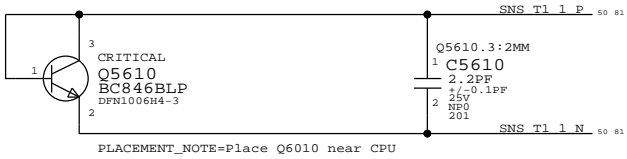
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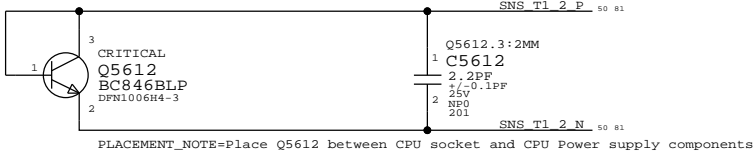


MLB Proximity

AC/DC Diode on supply



CPU Proximity

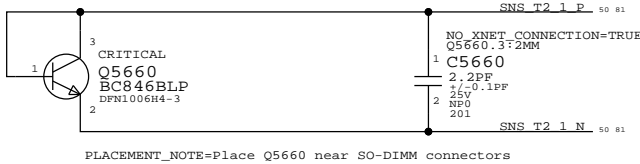


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode

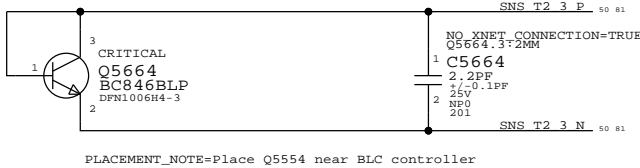
Temperature Sensor T2

Temperature Sensor T3: LCD Remote Sensor (Dev Only)

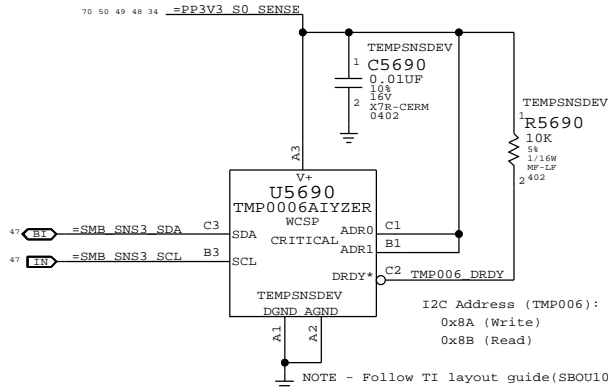
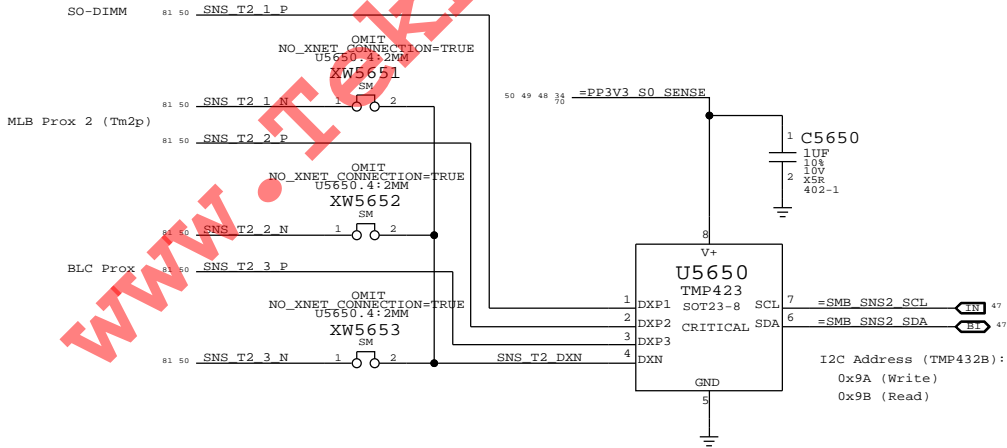
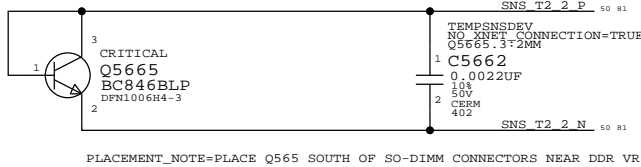
SO-DIMM Proximity




BLC Proximity



MLB Proximity



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
875-6433	1	BUMPER,U5690,D7	BUMPER_U5690	TEMPSNSDEV

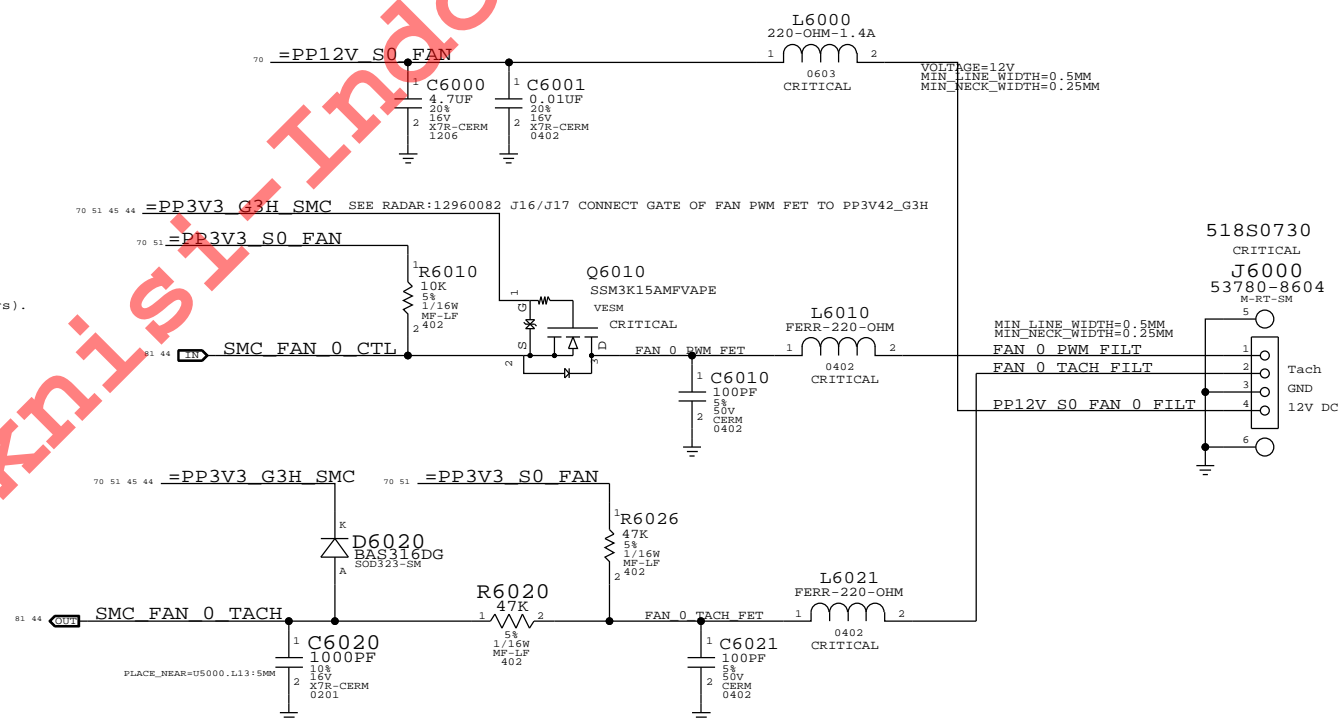
SYNC MASTER=J16 FIYIN		SYNC DATE=01/11/2013	
PAGE TITLE			
Temperature Sensors			
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		SIZE	D
		REVISION	12.4.0
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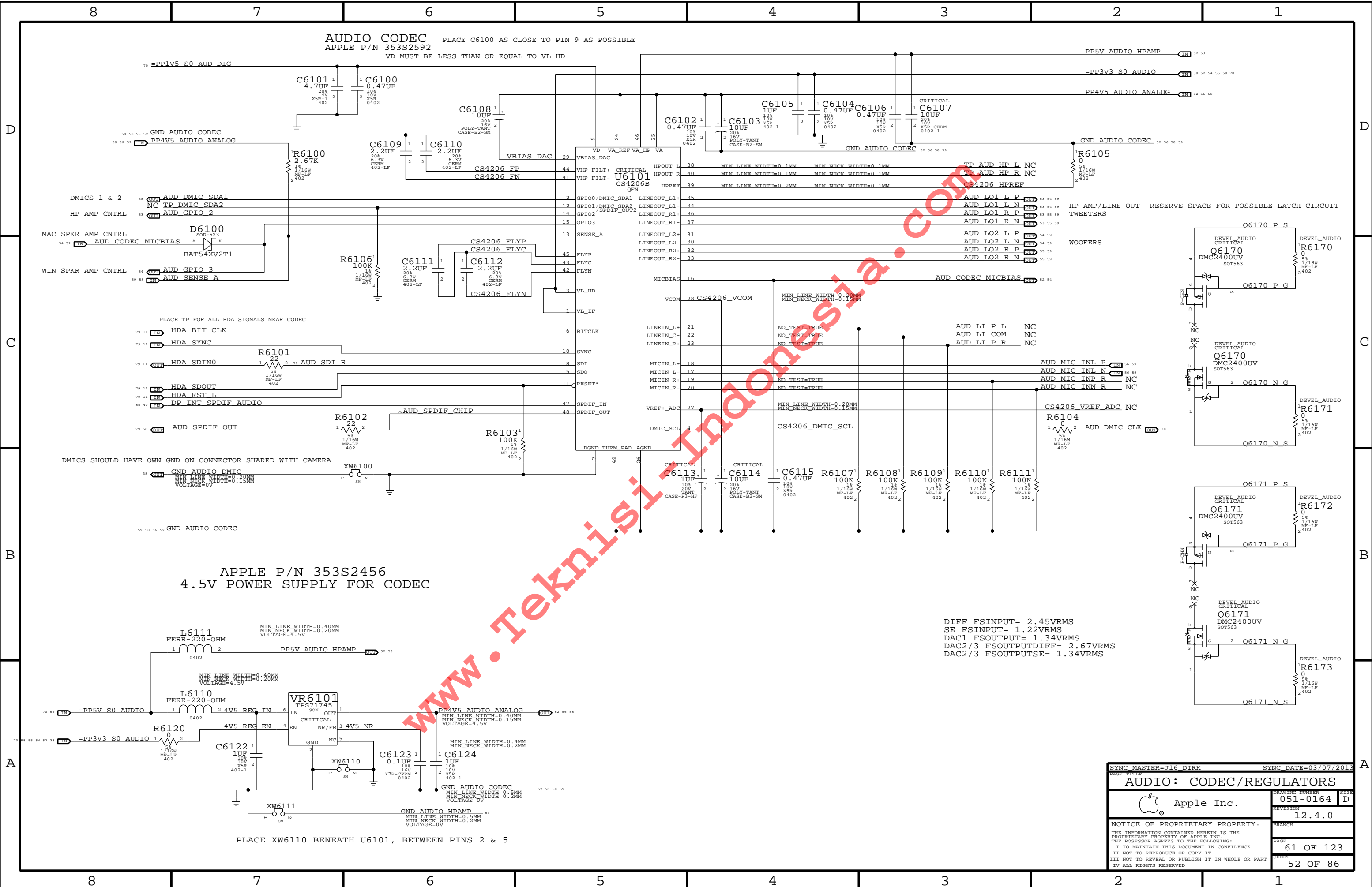
Note:

The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

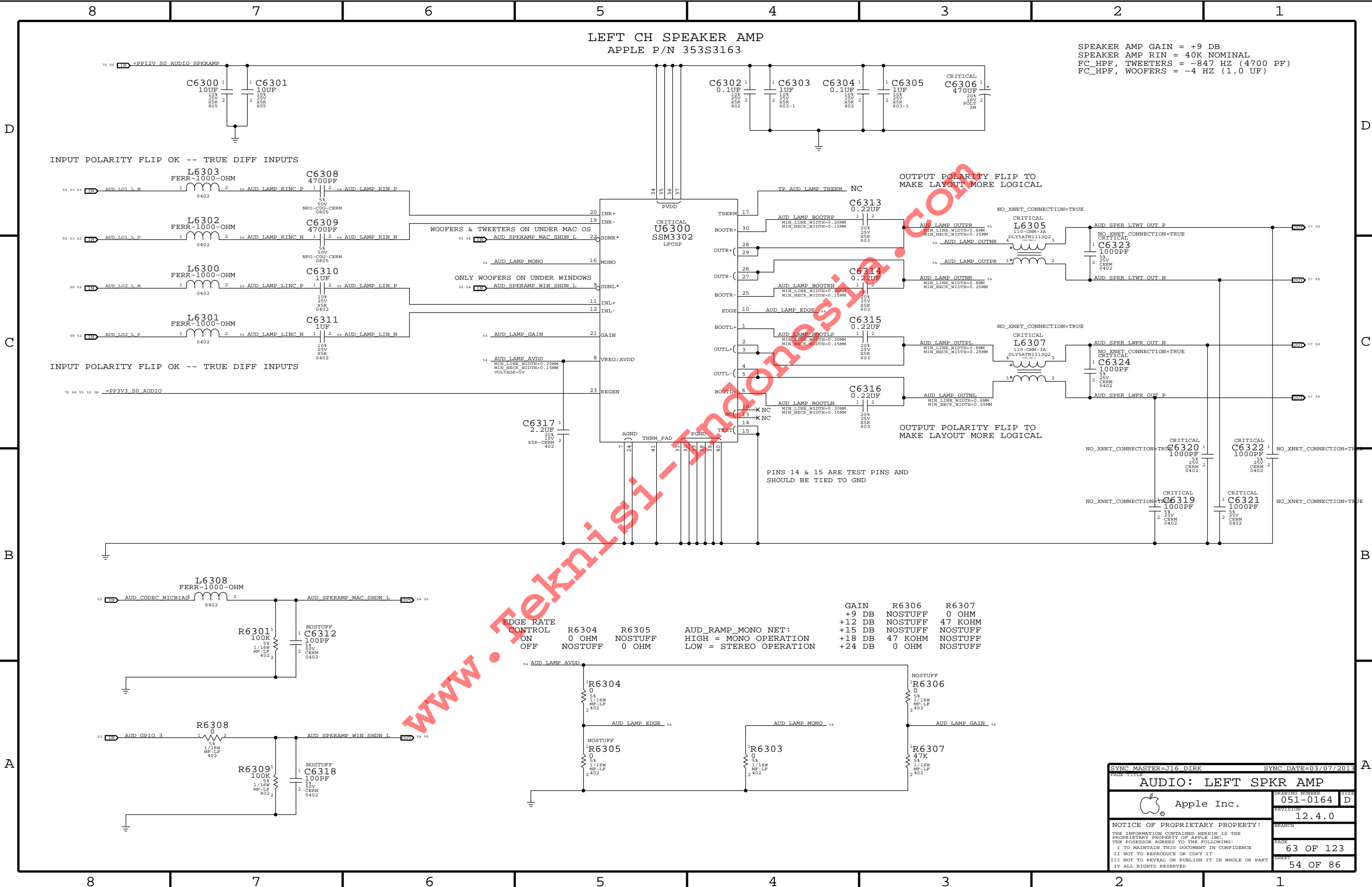
This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).





PAGE TITLE		PAGE NUMBER	
AUDIO: CODEC/REGULATORS		051-0164	
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LEFT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

OUTPUT POLARITY FLIP TO
MAKE LAYOUT MORE LOGICAL

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

OUTPUT POLARITY FLIP TO
MAKE LAYOUT MORE LOGICAL

PINS 14 & 15 ARE TEST PINS AND
SHOULD BE TIED TO GND


GAIN	R6306	R6307
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

EDGE RATE
CONTROL
ON
OFF

R6304
0 OHM
NOSTUFF

R6305
0 OHM
NOSTUFF

SYNC MASTER=J16 DIRK		SYNC DATE=03/07/2013	
PAGE TITLE			
AUDIO: LEFT SPKR AMP			
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		REVISION	12.4.0
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RIGHT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPFF, TWEETERS = ~847 HZ (4700 PF)
FC_HPFF, WOOFERS = ~4 HZ (1.0 UF)

D

D

C

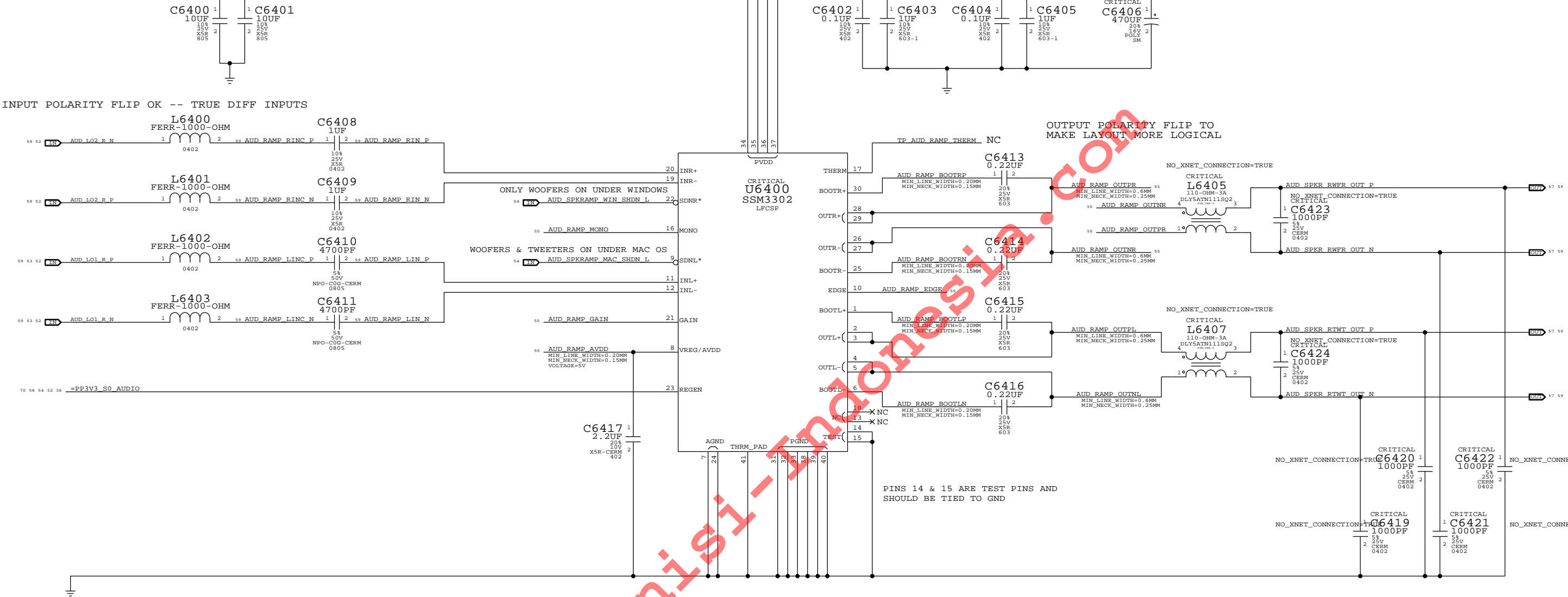
C

B

B

A

A



EDGE RATE CONTROL
ON
OFF

R6404
0 OHM
NOSTUFF

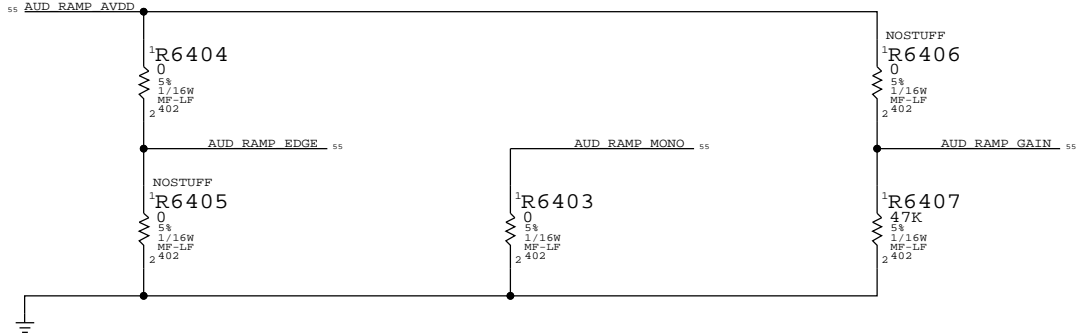
R6405
NOSTUFF
0 OHM


AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN
+9 DB
+12 DB
+15 DB
+18 DB
+24 DB

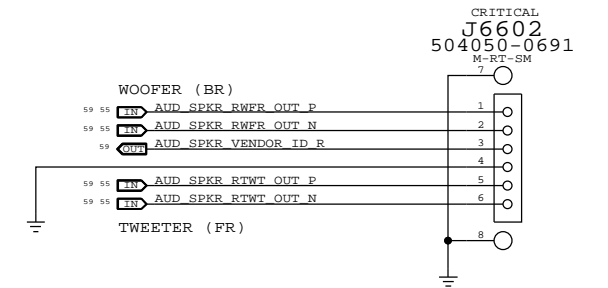
R6406
NOSTUFF
NOSTUFF
47 KOHM
0 OHM

R6407
0 OHM
NOSTUFF
NOSTUFF
NOSTUFF
NOSTUFF

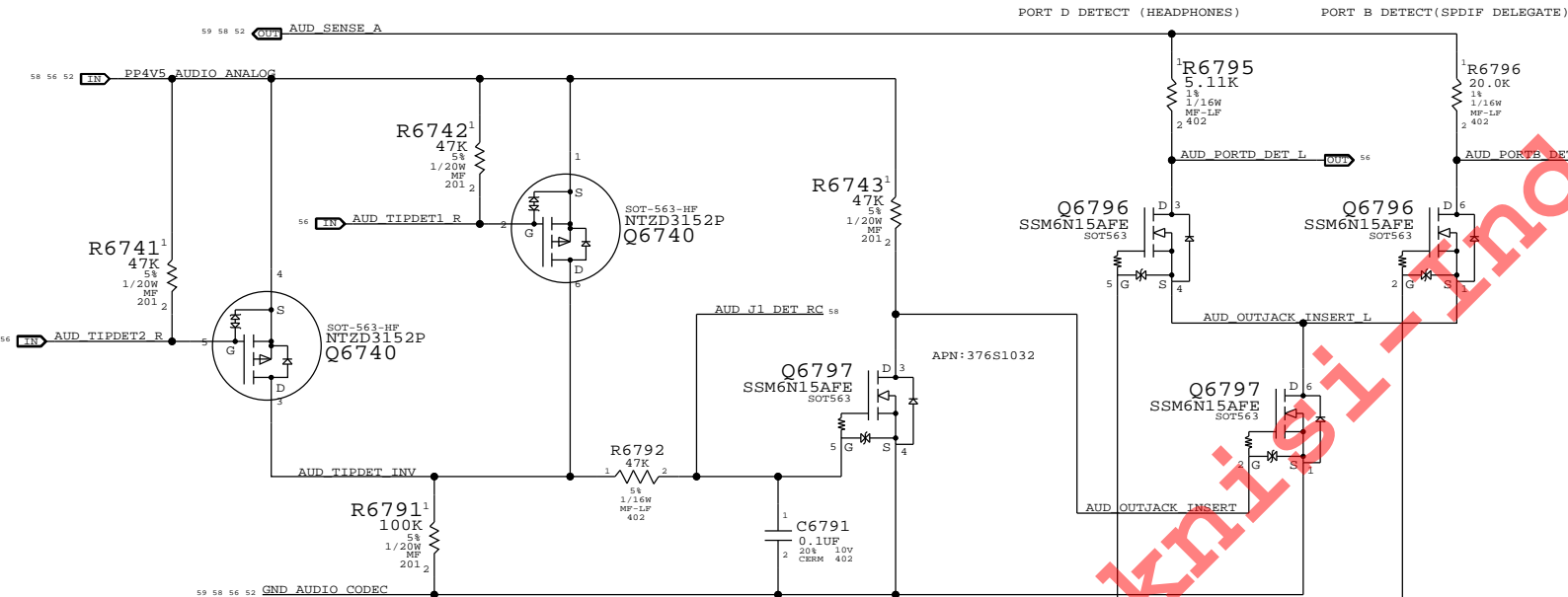
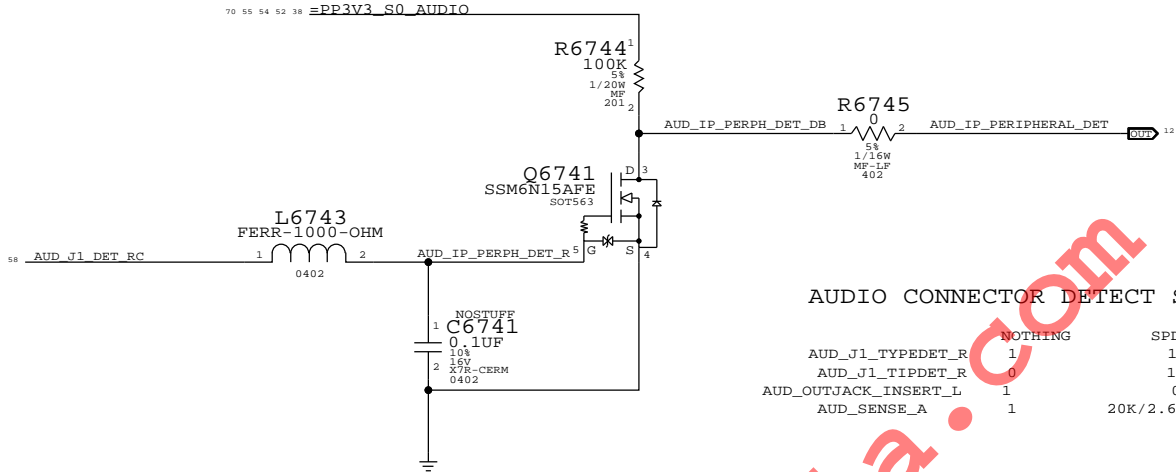


SYNC MASTER=J16 DIRK		SYNC DATE=03/07/2013	
PAGE TITLE			
AUDIO: RIGHT SPKR AMP			
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		051-0164	D
		REVISION	
		12.4.0	
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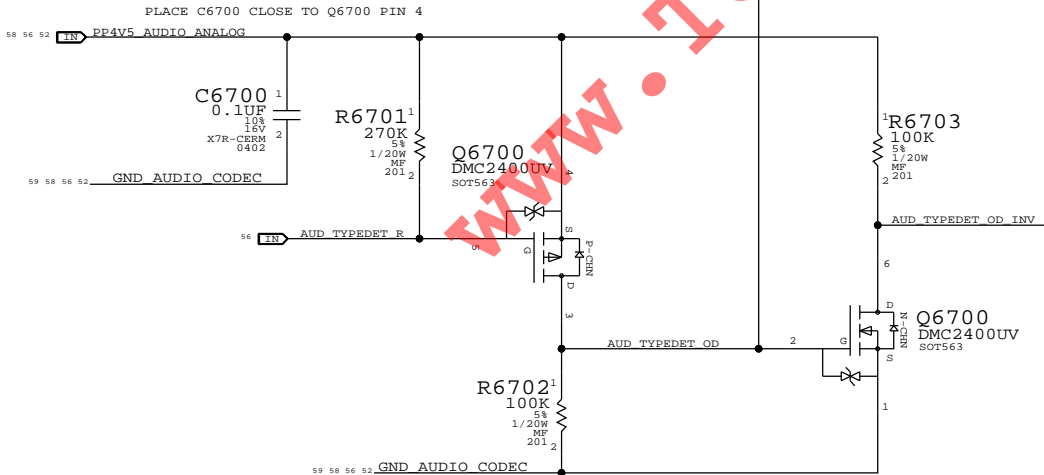
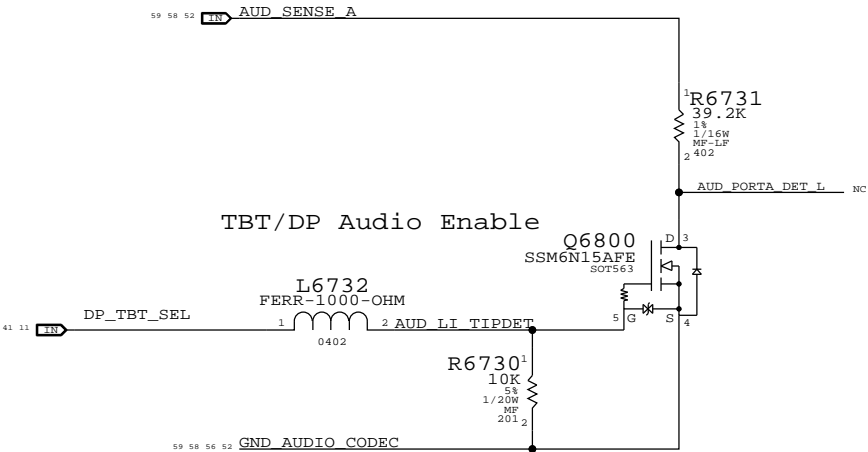
www.Teknisi-Indonesia.com

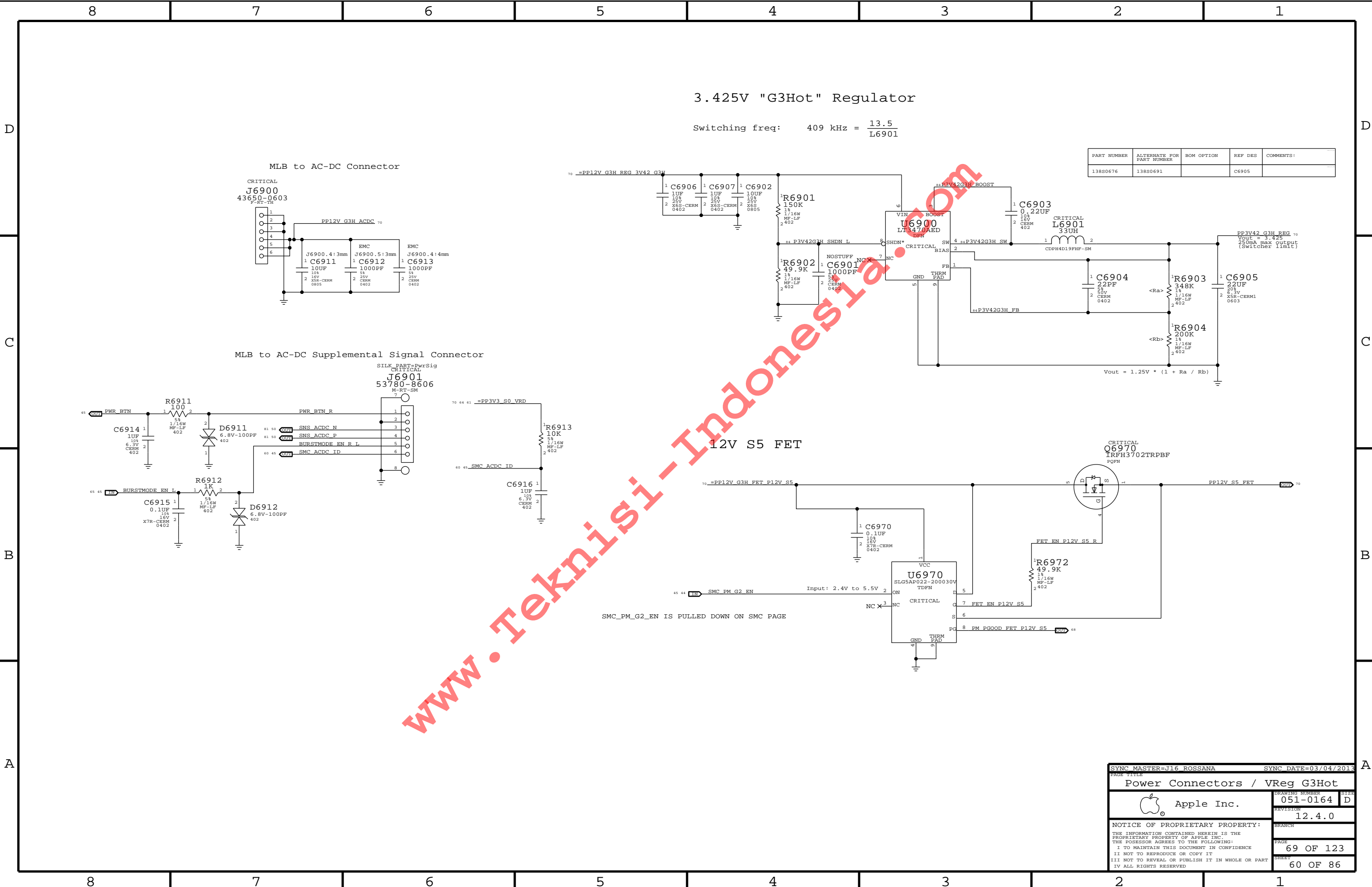


IPHS HS Detect Debounce CKT



Target Display Mode Detect






3.425V "G3Hot" Regulator

Switching freq: 409 kHz = $\frac{13.5}{L6901}$

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0676	138S0691		C6905	

CRITICAL
Q6970
IRFH3702TRPBF
PQFN

SYNC MASTER=J16 ROSSANA		SYNC DATE=03/04/2013	
PAGE TITLE			
Power Connectors /		VReg G3Hot	
	Apple Inc.		DRAWING NUMBER
			051-0164
			SIZE
			D
		REVISION	
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$$\text{Switching freq: } 403 \text{ kHz} = \frac{5 \text{ E10}}{\text{R7003}}$$

The schematic diagram illustrates the CPUVCC power plane for the i860. It features several key components and connections:

- Capacitors:**
 - C7031:** 68PF, 50V, COG-CERM 0402
 - C7030:** 0.0012UF, 10%, X7R-CERM 0402
 - R7037:** 1.82K, 1%, 1/16W, MF-LF 402
 - C7037:** 0.0012UF, 10%, 50V, CERM 0402
 - C7038:** 0.0012UF, 10%, 50V, CERM 0402
 - R7031:** 1K, 1%, 1/16W, MF-LF 402
 - R7032:** 750, 249, 1/16W, MF-LF 402
 - C7034:** 2.2NF, 10%, XSR-CERM 0201
 - R7033:** 7.15K, 1%, 1/16W, MF-LF 402
 - R7035:** 10, 1%, 1/16W, MF-LF 402
 - C7035:** 0.01UF, 10%, 16V, X7R-CERM 0402
 - R7036:** 2.67K, 1%, 1/16W, MF-LF 402
 - R7038:** 3.83K, 1%, 1/16W, MF-LF 402
- Resistors:**
 - R7030:** 7.15K, 1%, 1/16W, MF-LF 402
 - R7031:** 1K, 1%, 1/16W, MF-LF 402
 - R7032:** 750, 249, 1/16W, MF-LF 402
 - R7033:** 7.15K, 1%, 1/16W, MF-LF 402
 - R7034:** 787, 1%, 1/16W, MF-LF 402
 - R7035:** 10, 1%, 1/16W, MF-LF 402
 - R7036:** 2.67K, 1%, 1/16W, MF-LF 402
 - R7038:** 3.83K, 1%, 1/16W, MF-LF 402
- Connections:**
 - REG CPUVCC COMP:** Connected to C7031 and C7030.
 - CPUVCC COMP RC:** Connected to C7030 and R7030.
 - CPUVCC DVC:** Connected to R7037.
 - CPUVCC DVC RC:** Connected to R7037 and C7037.
 - To feedback:** Connected to C7037 and C7038.
 - REG CPUVCC FB:** Connected to C7037 and C7038.
 - CPUVCC FB RC:** Connected to C7038 and R7038.
 - AGND CPU:** Connected to R7038.
 - To PSI comp:** Connected to R7034 and C7034.
 - REG CPUVCC PSICOMP:** Connected to C7034.
 - To VSense:** Connected to R7035 and C7035.
 - REG CPUVCC VSEN:** Connected to C7035.
 - To HF comp:** Connected to R7036 and C7036.
 - REG CPUVCC HFCOMP:** Connected to C7036.

The schematic diagram illustrates the CPU power supply section, showing the connection of the CPU VCCSENSE pins to the power supply rails and the voltage sense pins to the voltage sense pins.

Power Supply Section:

- Input:** The input is connected to the CPU VCCSENSE P pin (pin 83) and the CPU VCCSENSE R pin (pin 61).
- Resistors:** A 1K resistor (R7042) is connected between the input and the CPU VCCSENSE P pin. A 1K resistor (R7047) is connected between the input and the CPU VCCSENSE R pin.
- Capacitors:** A 1/16W MF-LF 402 capacitor (C7048) is connected between the CPU VCCSENSE P pin and ground. A 1/16W MF-LF 402 capacitor (C7046) is connected between the CPU VCCSENSE R pin and ground.
- Grounding:** The input is connected to ground (AGND_CPU) via a 1/16W MF-LF 402 capacitor (C7048).

Voltage Sense Section:

- Input:** The input is connected to the CPU VCCSENSE P pin (pin 83) and the CPU VCCSENSE R pin (pin 61).
- Resistors:** A 1K resistor (R7042) is connected between the input and the CPU VCCSENSE P pin. A 1K resistor (R7047) is connected between the input and the CPU VCCSENSE R pin.
- Capacitors:** A 1/16W MF-LF 402 capacitor (C7048) is connected between the CPU VCCSENSE P pin and ground. A 1/16W MF-LF 402 capacitor (C7046) is connected between the CPU VCCSENSE R pin and ground.
- Grounding:** The input is connected to ground (AGND_CPU) via a 1/16W MF-LF 402 capacitor (C7048).

Legend:

- NO_XNET_CONNECTION=TRUE:** This label is present on the input lines, indicating that the XNET connection is not used.
- REG CPUVCC VSEN:** This label is present on the output lines, indicating that the voltage sense pins are connected to the voltage sense pins.

[illegible]

5V REG VCC U7000

R7090
1K
5%
1/16W
MF-LP
402

RT7090
6.8K
0603

C7090
0.1uF
104
16V
X7R-CERM
0402

REG CPUVCC TM

AGND CPU

The schematic diagram illustrates the CPU power plane, showing the connections between the CPU pins and the power regulators and decoupling capacitors. The components are organized into two rows of four columns each.

Top Row Components:

- Column 1:** REG_VCC_U7000 (pin 83) connects to the input of R7001 (340K, 1% tolerance, 1/20W, 201 package). The output of R7001 connects to the input of R7007 (NOSTUFF, 0% tolerance, 1/20W, 201 package).
- Column 2:** REG_CPUVCC_IMX (pin 61) connects to the input of R7003 (124K, 1% tolerance, 1/20W, 201 package).
- Column 3:** REG_CPUVCC_FVID (pin 61) connects to the input of R7005 (150K, 1% tolerance, 1/20W, 201 package).
- Column 4:** REG_CPUVCC_TM5 (pin 61) connects to the input of R7007 (NOSTUFF, 0% tolerance, 1/20W, 201 package).

Bottom Row Components:

- Column 1:** REG_CPUVCC_NPSI (pin 83) connects to the input of R7002 (95.3K, 1% tolerance, 1/20W, 201 package).
- Column 2:** R7002 connects to the input of R7004 (NOSTUFF, 0% tolerance, 1/20W, 201 package).
- Column 3:** R7004 connects to the input of R7006 (147K, 1% tolerance, 1/20W, 201 package).
- Column 4:** R7006 connects to the input of R7008 (249K, 1% tolerance, 1/20W, 201 package).

Output and Decoupling:

- The output of R7008 connects to the input of C7001 (0.047UF, 10% tolerance, X58 package, 0201 package).
- The output of C7001 connects to the AGND_CPU pin (pin 61).

70 64 60 =PP3V3_S0_VDD

1R7098
10K
5%
1/16W
MF-LF
2402

61 REG_CPUVCC_PGOOD = PM_PGOOD_REG_CPUVCC_S0 0100 65

61 REG_CPIUVCC_VRHOT_L

R7093

1/16W 402

CPU_PROCHOT_L

C7091


47PF

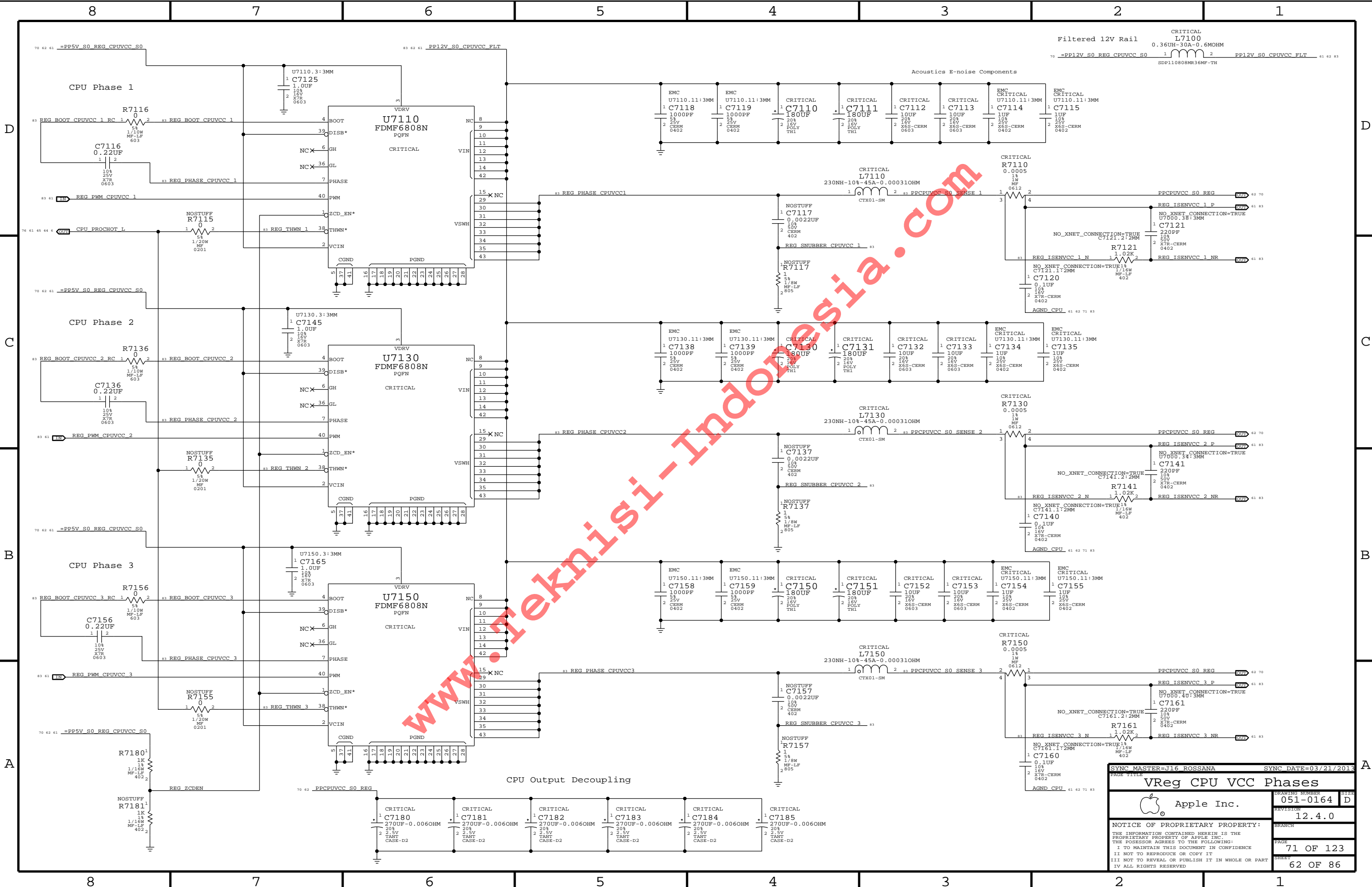
20V


402

Per Intel Shark Bay PDG

J16: 3PHASE				
J17: 4PHASE				
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
118S0311	1	RES, 340K, 201	R7001	CPUVCC:3PHASE
118S0116	1	RES, 158K, 201	R7001	CPUVCC:4PHASE
118S0575	1	RES, 95.3K, 201	R7002	CPUVCC:3PHASE
118S0380	1	RES, 44.2K, 201	R7002	CPUVCC:4PHASE
114S0206	1	RES, 750 OHM, 402	R7032	CPUVCC:3PHASE
114S0211	1	RES, 845 OHM, 402	R7032	CPUVCC:4PHASE
114S0179	1	RES, 402 OHM, 402	R7050	CPUVCC:3PHASE
114S0184	1	RES, 453 OHM, 402	R7050	CPUVCC:4PHASE

SYMC MASTER=J16 ROSSANA		SYMC DATE=03/21/2013	
PAGE TITLE			
VReg CPU VCC Cntl			
	Apple Inc.		DRAWING NUMBER 051-0164
			SIZE D
		REVISION 12.4.0	
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		SHEET 61 OF 86	



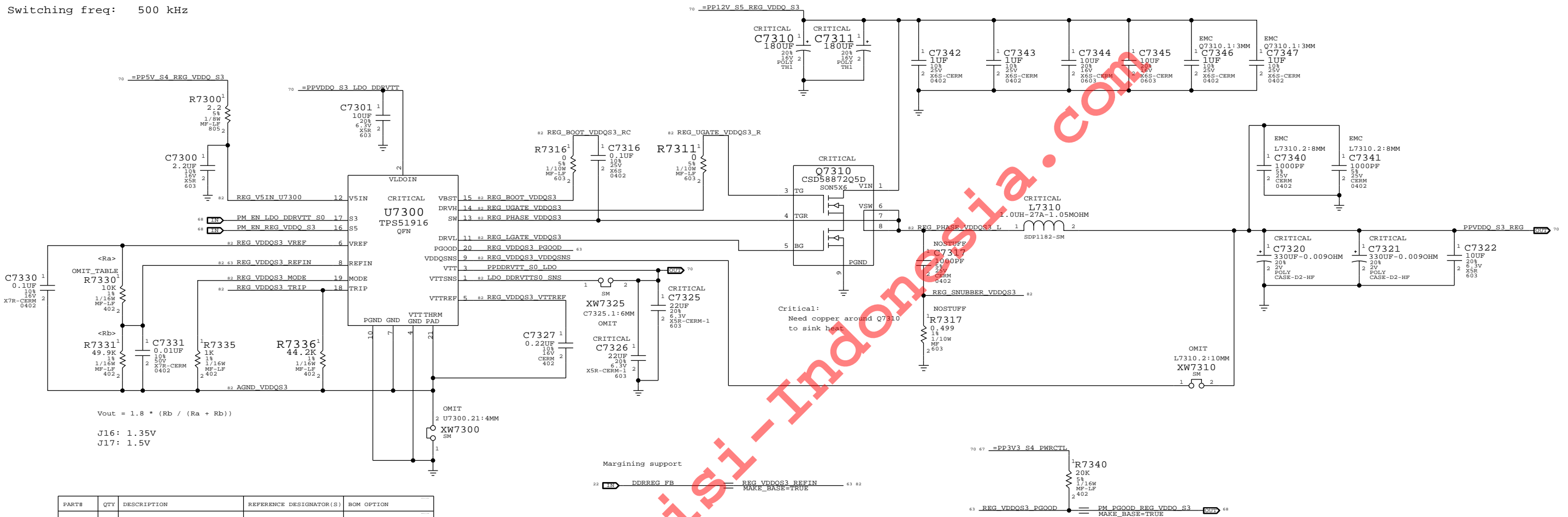
SYNC MASTER=J16 ROSSANA		SYNC DATE=03/21/2013	
PAGE TITLE		VReg CPU VCC Phases	
 Apple Inc.		DRAWING NUMBER	051-0164
		REVISION	12.4.0
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VDDQ (1.5V / 1.35V) S3 Regulator

OC trip point: $30.4 \text{ A VDDQ} = \frac{R7336}{8 \text{ E5} * R_{ds}(Q7310)} + \frac{0.65625}{L7310 * f(\text{switch})}$

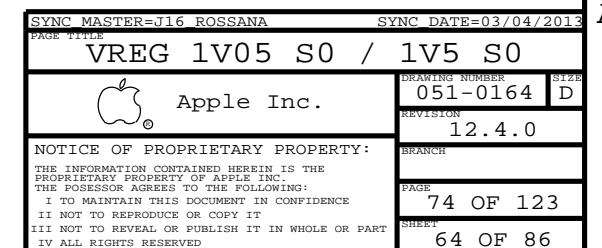
3 A VTT (FIXED)
10 mA VTTREF (FIXED)

Switching freq: 500 kHz



D

C

B

3.3V S5 Regulator

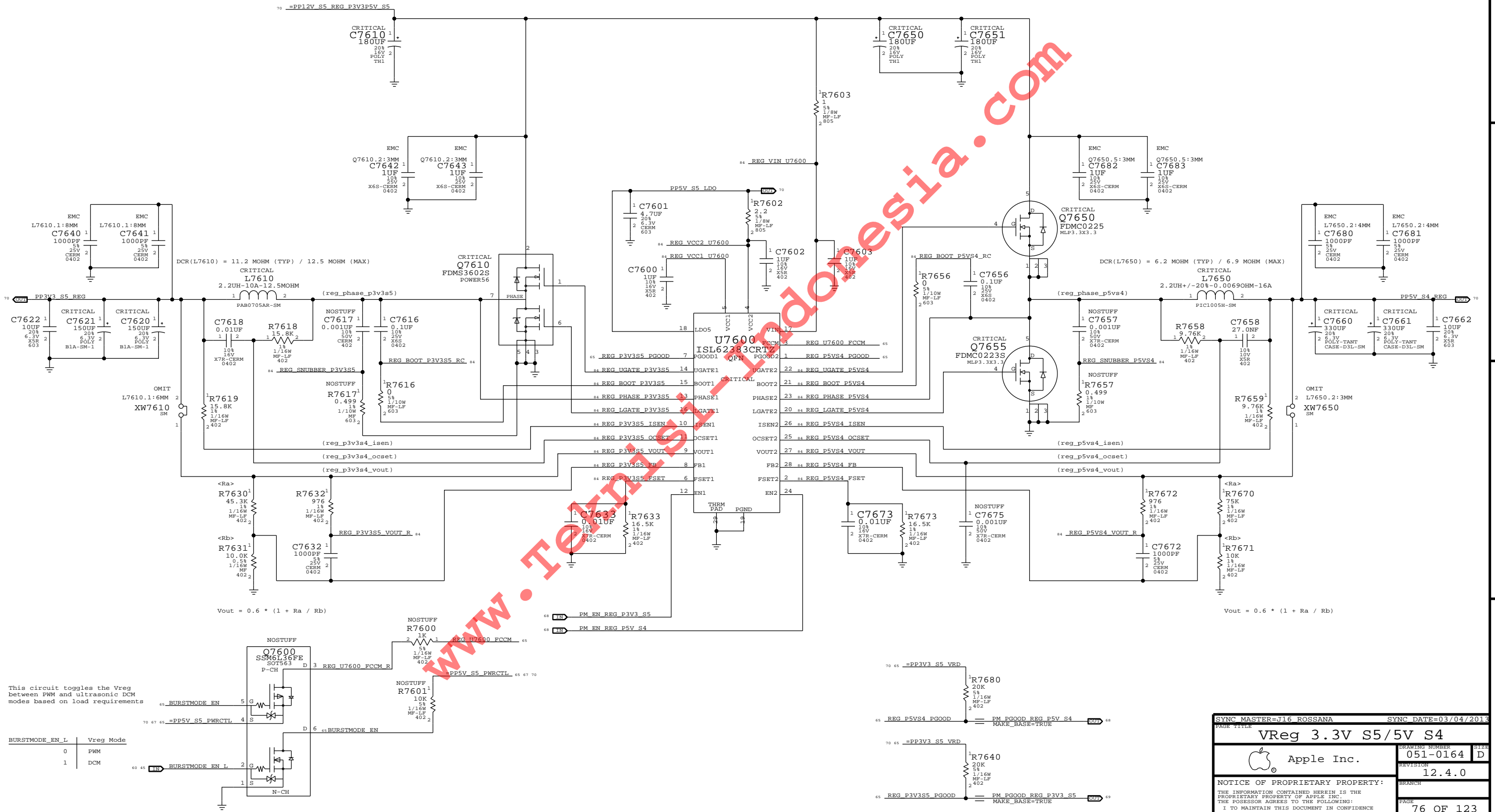
OC trip point: $12.5 \text{ A} = \frac{R7618 * 10 \text{ E-6}}{\text{DCR}(L7610)}$


Switching freq: $356 \text{ kHz} = \frac{1}{170 \text{ E-12} * R7633}$

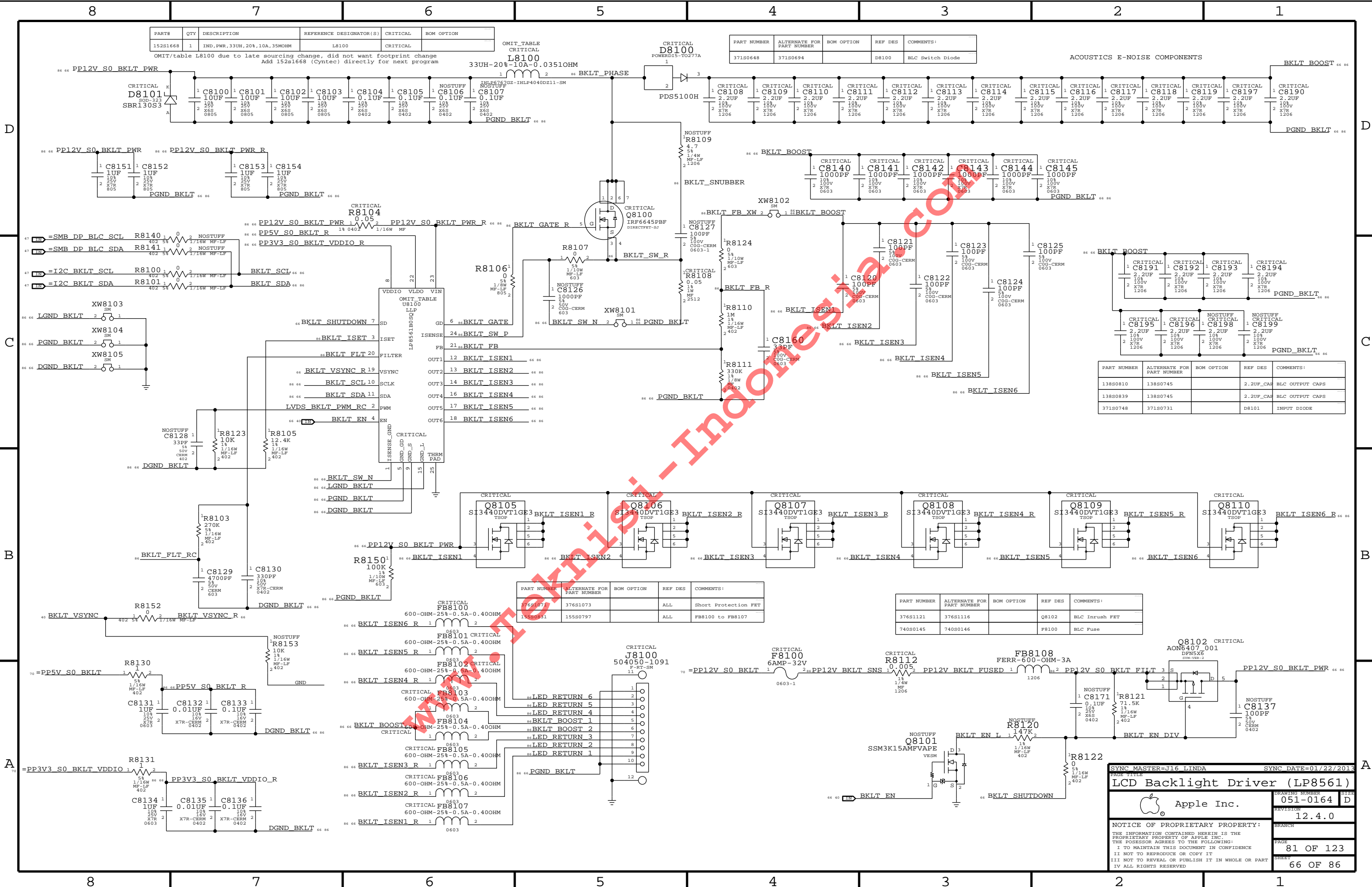
5V S4 Regulator

OC trip point: $14.1 \text{ A} = \frac{R7658 * 10 \text{ E-6}}{\text{DCR}(L7650)}$

Switching freq: $356 \text{ kHz} = \frac{1}{170 \text{ E-12} * R7673}$



SYNC MASTER=J16 ROSSANA		SYNC DATE=03/04/2013	
PAGE TITLE			
VReg 3.3V S5/5V S4			
	DRAWING NUMBER		051-0164
	REVISION		12.4.0
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SHEET			65 OF 86



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
-------	-----	-------------	-------------------------	----------	------------

OMIT/table L8100 due to late sourcing change, did not want footprint change
Add 152s1668 (Cyntec) directly for next program

CRITICAL
L8100
33UH-20%-10A-0.03510HM

CRITICAL
D8100
POWERD15-T0277A

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
-------------	---------------------------	------------	---------	-----------

ACOUSTICS E-NOISE COMPONENTS

BKLT BOOST

PGND BKLT

CRITICAL
R8104
0.05

CRITICAL
Q8100
IRF6645PBF

CRITICAL
Q8105
SI3440DVT1GE3

CRITICAL
Q8106
SI3440DVT1GE3

CRITICAL
Q8107
SI3440DVT1GE3

CRITICAL
Q8108
SI3440DVT1GE3

CRITICAL
Q8109
SI3440DVT1GE3

CRITICAL
Q8110
SI3440DVT1GE3

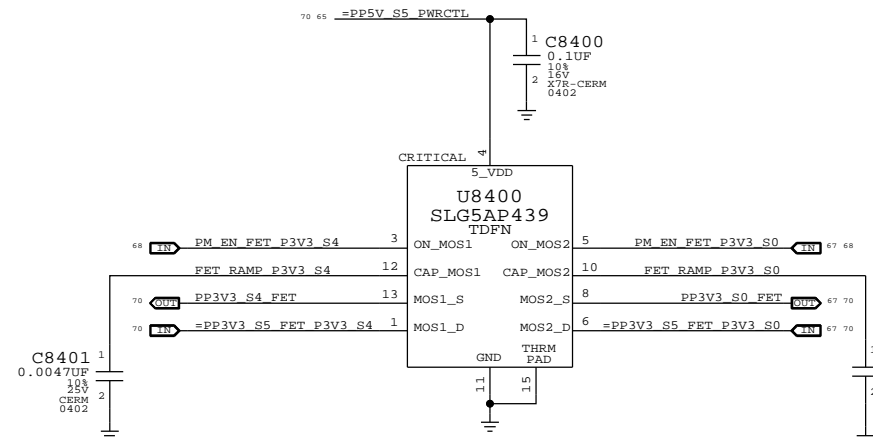
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0810	138S0745		2.2UF_CAP	BLC OUTPUT CAPS
138S0839	138S0745		2.2UF_CAP	BLC OUTPUT CAPS
371S0748	371S0731		D8101	INPUT DIODE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1071	376S1073		ALL	Short Protection FET
155S0831	155S0797		ALL	FB8100 to FB8107

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1121	376S1116		Q8102	BLC Inrush FET
740S0145	740S0146		F8100	BLC Fuse

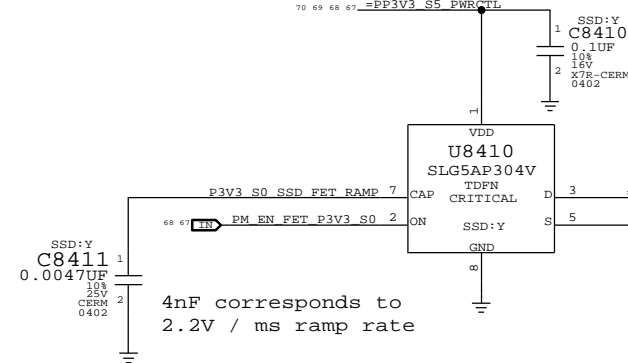
SYNC MASTER=J16 LINDA		SYNC DATE=01/22/2013	
PAGE TITLE		DRAWING NUMBER	
LCD Backlight Driver (LP8561)		051-0164	
Apple Inc.		REVISION	12.4.0
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3.3V S4 FET

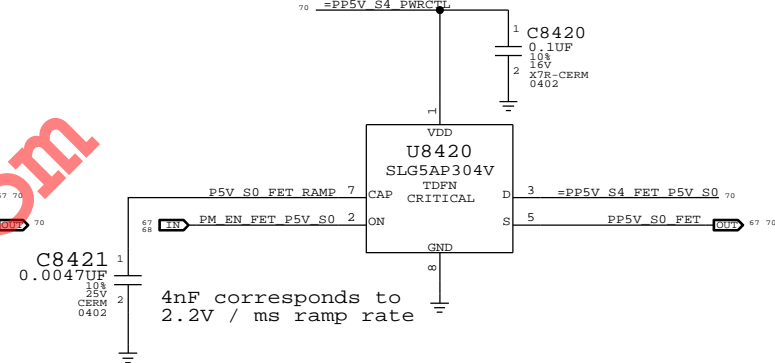


3.3V S0 FET

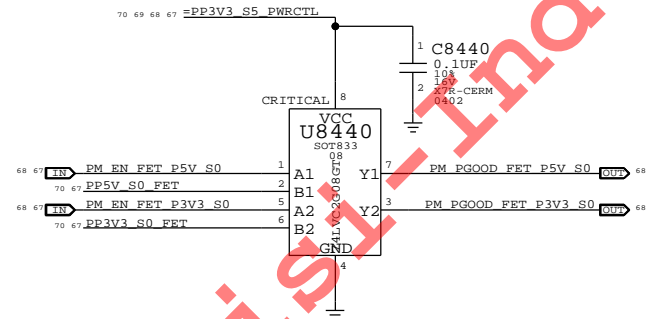
3V3 S0 SSD



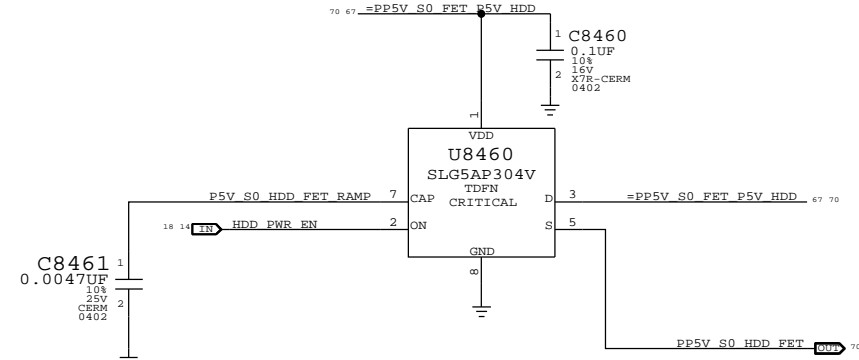
5V S0 FET



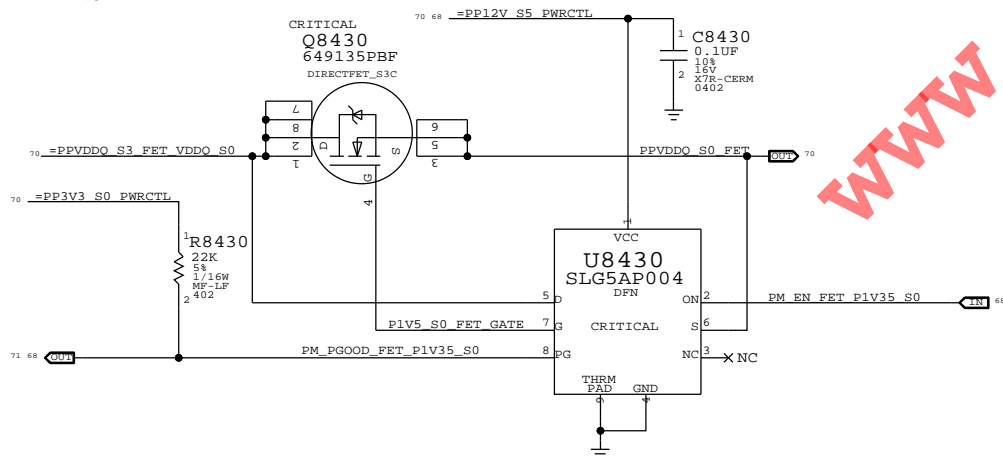
5V / 3V3 S0 PGOODs



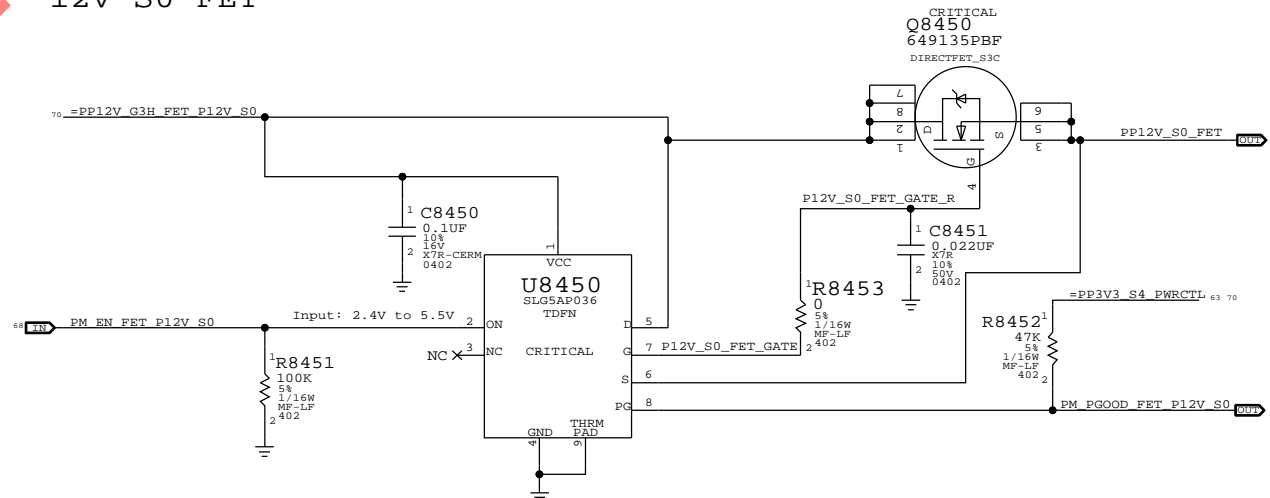
5V HDD FET



VDDQ S0 FET

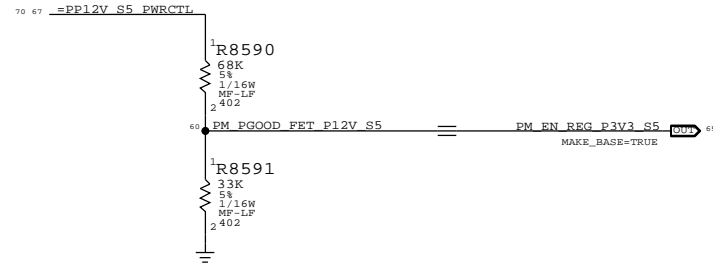


12V S0 FET

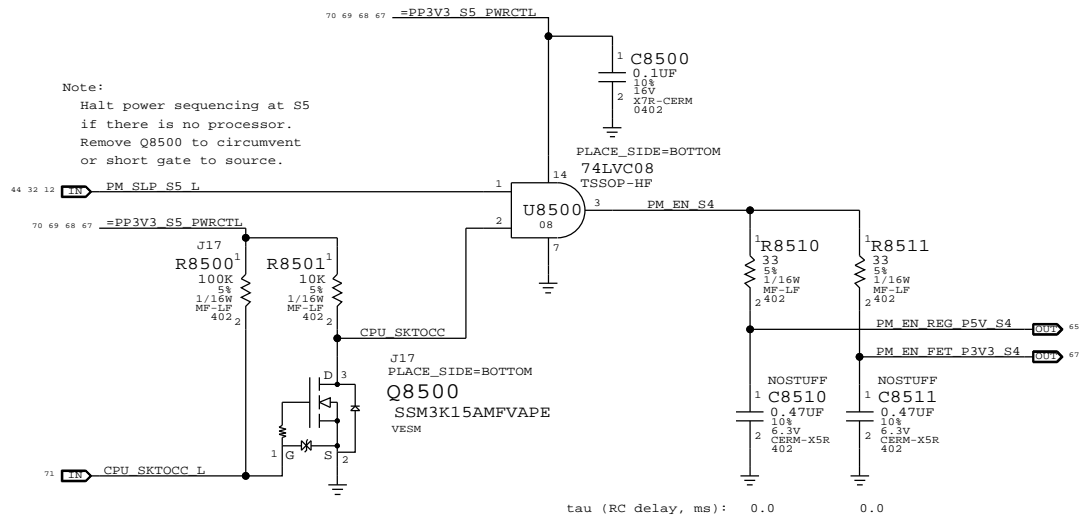


SYNC MASTER=J16 MAX		SYNC DATE=02/11/2013	
PAGE TITLE		FET-Controlled S0 and S4	
Apple Inc.		DRAWING NUMBER	051-0164
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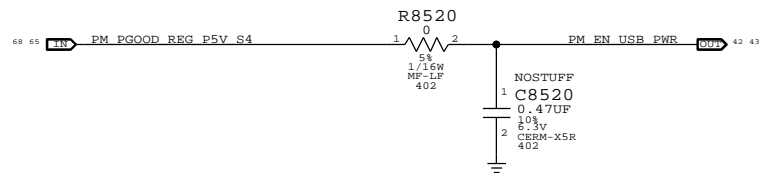
S5 Enable



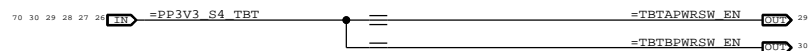
S4 Enables



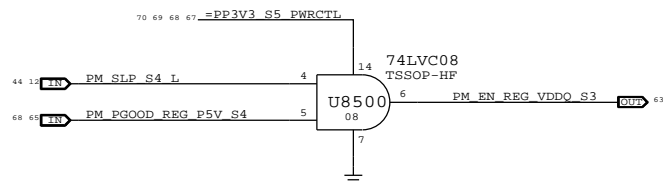
S4 USB Enable



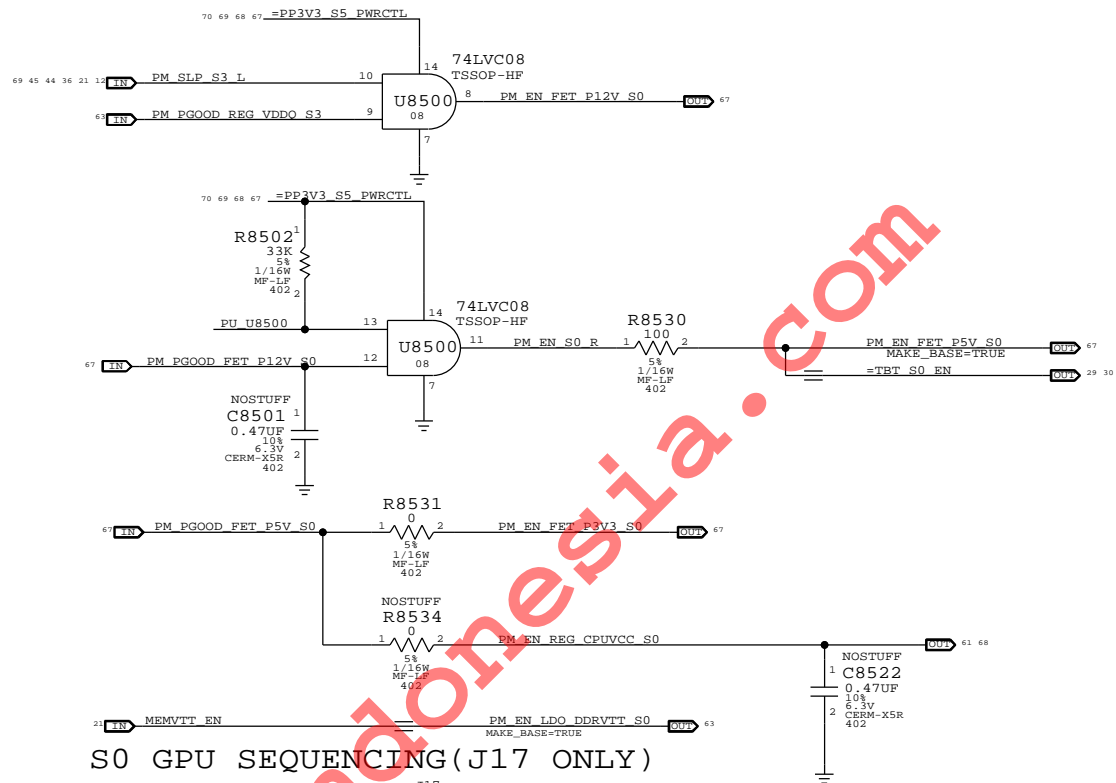
S4 TBT S4 Port Enable



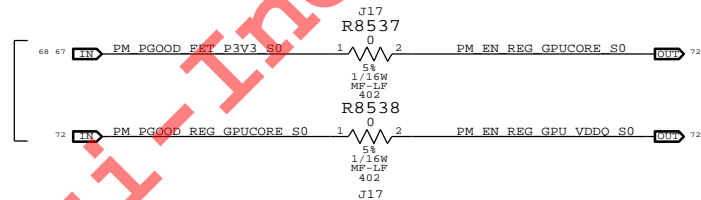
S3 VDDQ Enable



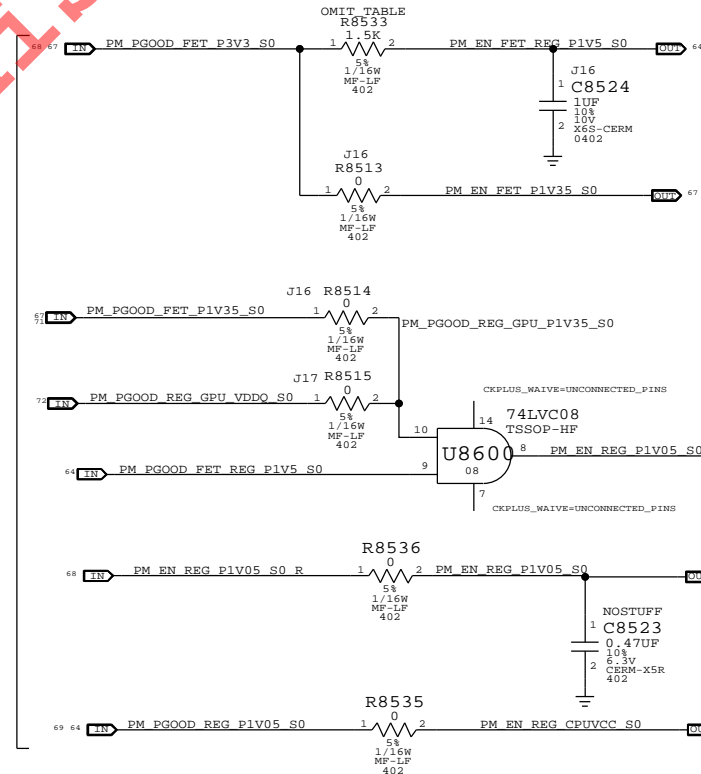
S0 Enables



S0 GPU SEQUENCING (J17 ONLY)



S0 PCH Sequencing




PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0070	1	RES,1.5K,0402,5%	R8533	J16
116S0004	1	RES,00HM,0402,5%	R8533	J17

Rail definitions

Platform: All processor non-Core and non-Graphics (5 V, 3.3 V, 1.5 V, 1.05V for PCH/TBT/GPU)
Uncore: VDDQ

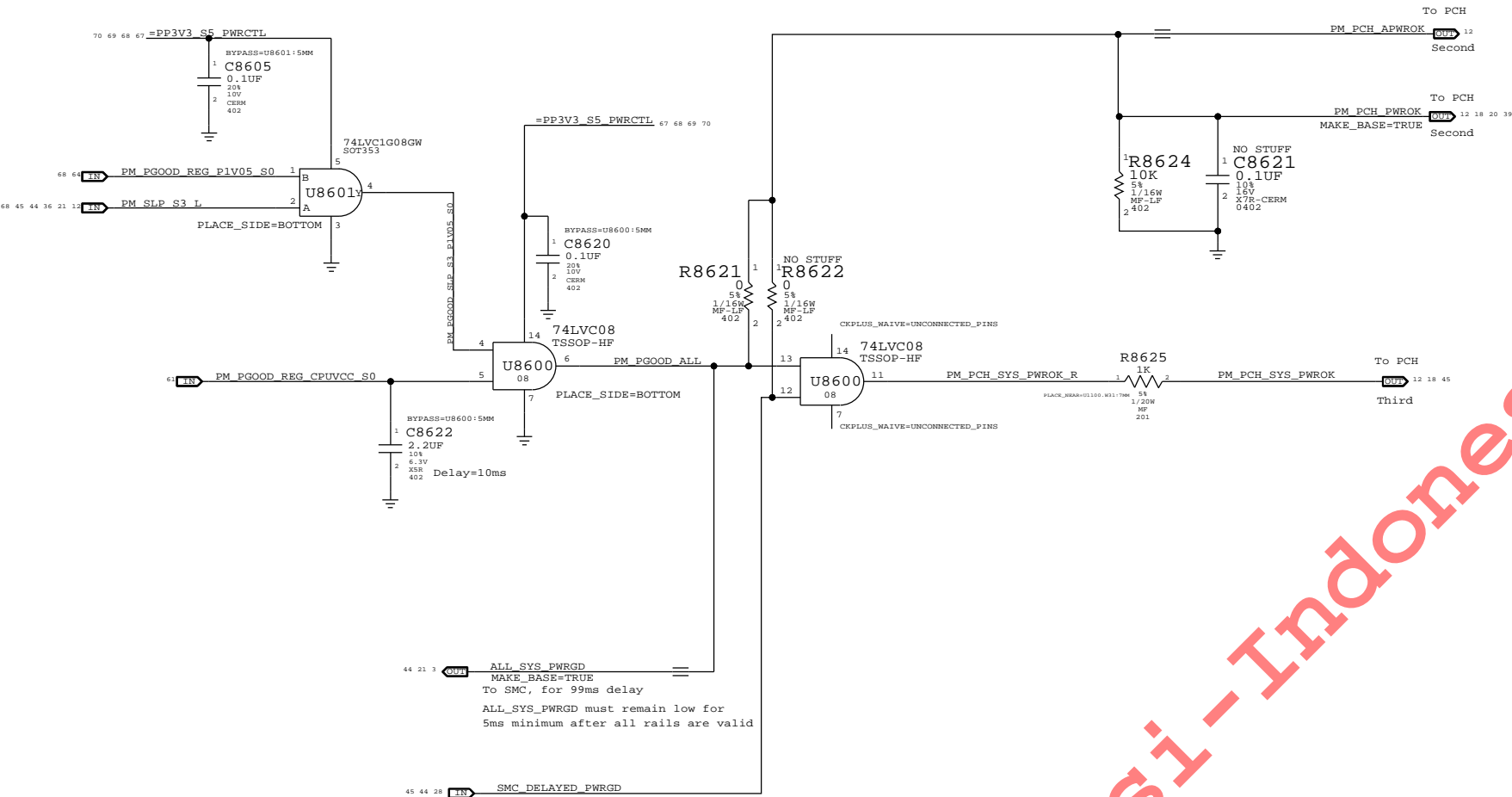
Notes on sequencing requirements

- Intel:
- No hard specification on platform rails
 - SMC guarantees timing on PCH DPWROK and PWROK
 - VCC3_3 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC3V3 ramping to 2.6V
 - VCC1_5 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC1V5 ramping to 1.35V
 - VCC may power down before VCC3_3, VCC3_3 must ramp down to 2.6V within 35ms
 - VCC may power down before VCC1_5, VCC1_5 must ramp down to 1.35V within 35ms
- NVIDIA:
- 3V3_S0 must ramp first
 - VDDQ MUST RAMP AFTER GPU_CORE
 - PEX_VDD with IFPC/D/E/F_IOVDD (1.05V) must ramp after VDDQ
 - All rails must reach their target voltages in more than 40 uS

SYNC MASTER=J16 AARON		SYNC DATE=02/21/2013	
PAGE TITLE			
PM Regulator Enables			
 Apple Inc.		DRAWING NUMBER	051-0164
		SIZE	D
		REVISION	12.4.0
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ALL_SYS_PWRGD,PCH_PWROK & SYS_PWROK Generation

PCH Power Goods

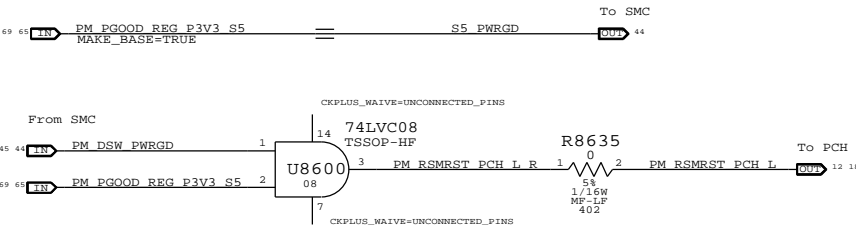


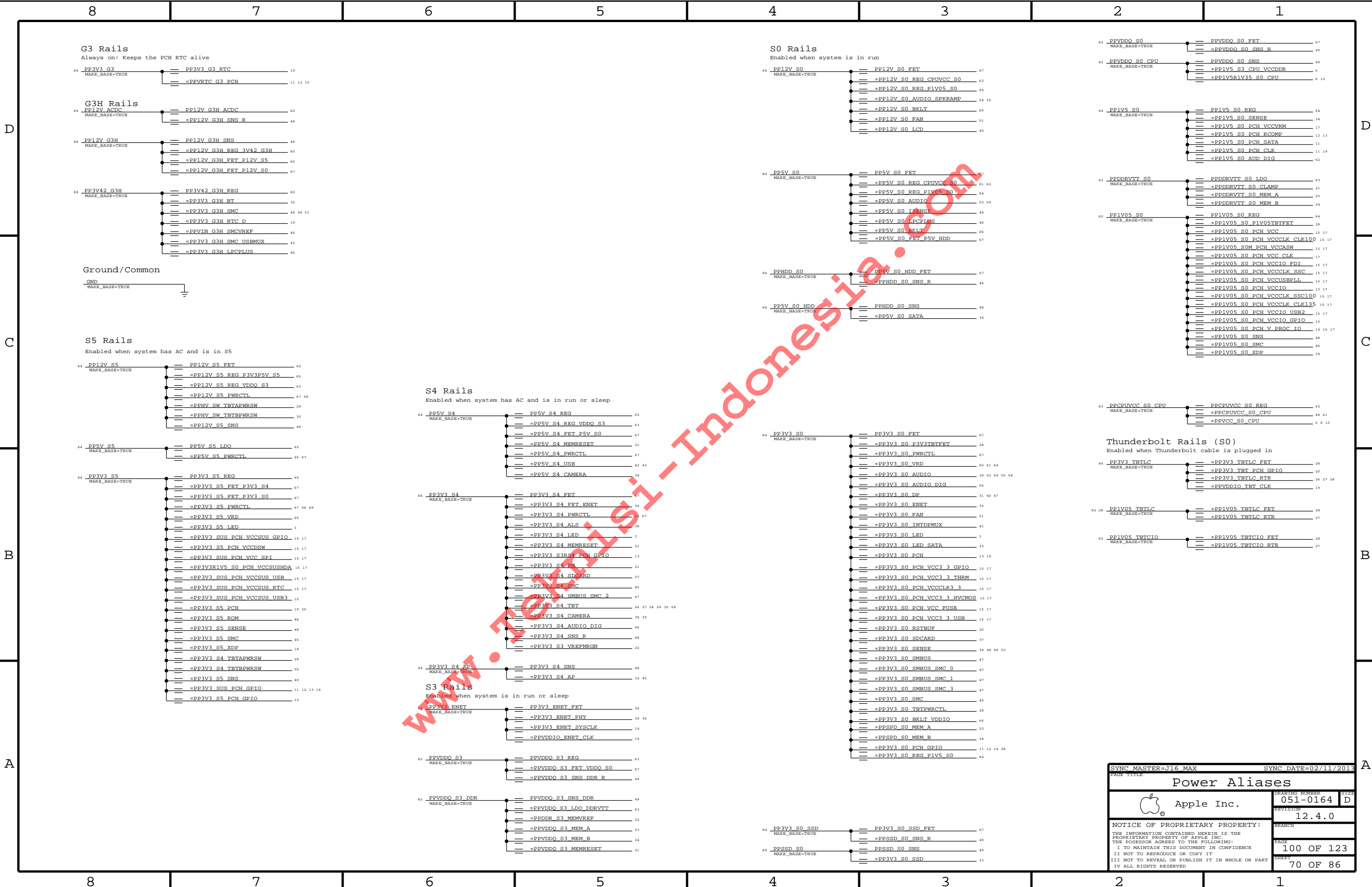
Resume Reset

Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8
Note:
The iMac J16/J17 designs does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V
to allow PCH to switch suspend well to battery without excessive loading

Method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.
RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.






SYNC MASTER=J16 MAX

SYNC DATE=02/11/2013

Power Aliases

Apple Inc.

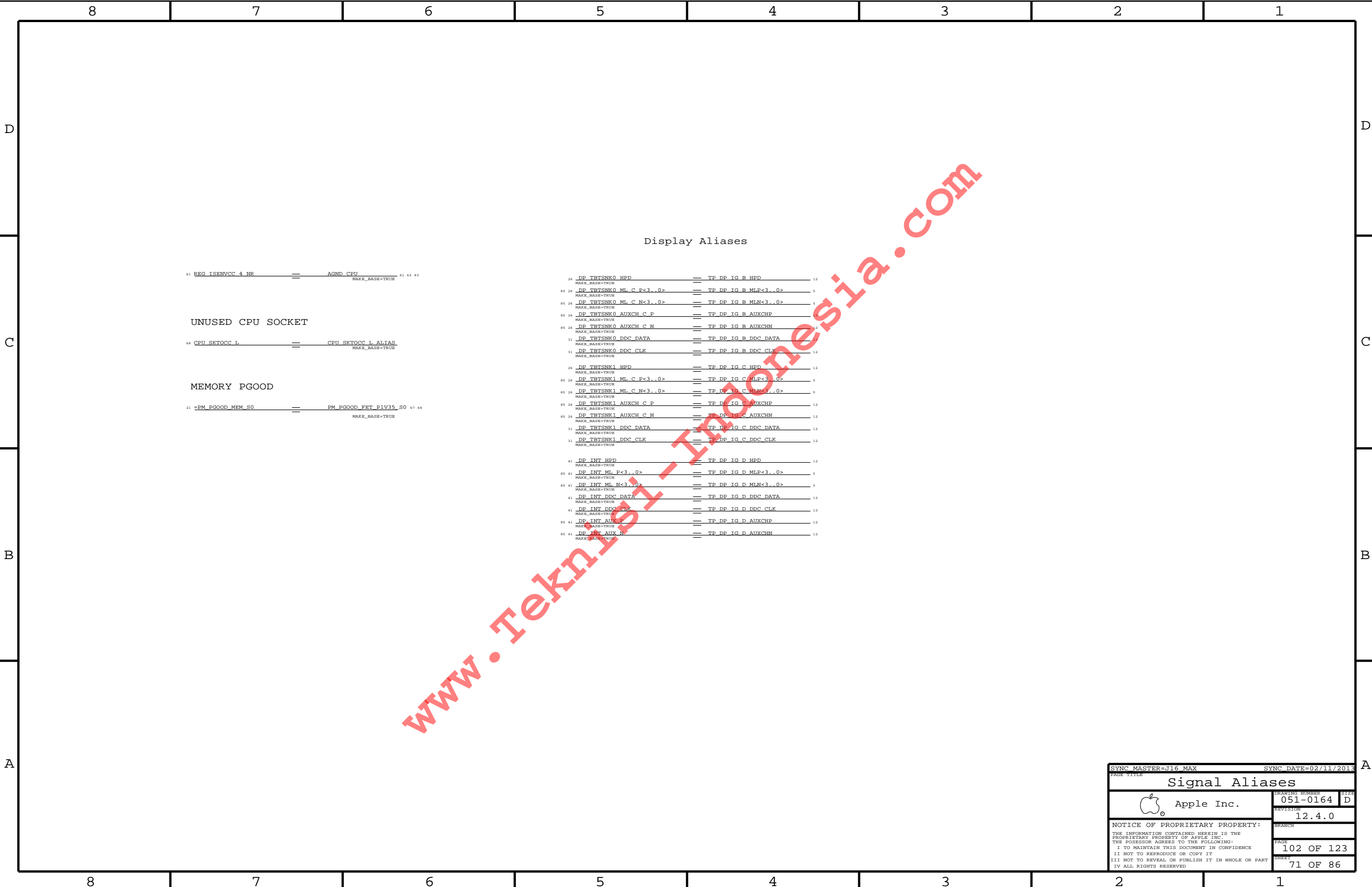
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DRAWING NUMBER
051-0164

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8	7	6	5	4	3	2	1
CPU Reserved		UNUSED GRAPHICS ALIASES					
78 18 6 CPU CFG<15..12> == TP_CPU_CFG<15..12> MAKE_BASE=TRUE		20 TP_GPU_RESET_L == NC_TP_GPU_RESET_L MAKE_BASE=TRUE NO_TEST=TRUE					
CPU Memory		UNUSED THUNDERBOLT ALIASES					
75 MEM_A_CLK_N<2..3> == NC_MEM_A_CLKN<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		26 TP_TBT_PCIE_RESETO_L == NC_TBT_PCIE_RESETO_L MAKE_BASE=TRUE NO_TEST=TRUE					
75 MEM_A_CLK_P<2..3> == NC_MEM_A_CLKP<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		26 TP_TBT_PCIE_RESET1_L == NC_TBT_PCIE_RESET1_L MAKE_BASE=TRUE NO_TEST=TRUE					
75 MEM_A_CS_L<2..3> == NC_MEM_A_CS_L<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		26 TP_TBT_PCIE_RESET2_L == NC_TBT_PCIE_RESET2_L MAKE_BASE=TRUE NO_TEST=TRUE					
75 MEM_A_CKE<2..3> == NC_MEM_A_CKE<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		26 TP_TBT_PCIE_RESET3_L == NC_TBT_PCIE_RESET3_L MAKE_BASE=TRUE NO_TEST=TRUE					
75 MEM_B_CLK_N<2..3> == NC_MEM_B_CLKN<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		26 TP_TBT_THERM_DP == NC_TBT_THERM_DP MAKE_BASE=TRUE NO_TEST=TRUE					
75 MEM_B_CLK_P<2..3> == NC_MEM_B_CLKP<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		UNUSED VREG ALIASES					
75 MEM_B_CS_L<2..3> == NC_MEM_B_CS_L<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		61 REG_PWM_CPUVCC_4 == NC_REG_PWM_CPUVCC_4 MAKE_BASE=TRUE NO_TEST=TRUE					
75 MEM_B_CKE<2..3> == NC_MEM_B_CKE<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		61 REG_ISENVC_4_P == NC_REG_ISENVC_4_P MAKE_BASE=TRUE NO_TEST=TRUE					
75 MEM_A_ODT<2..3> == NC_MEM_A_ODT<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		UNUSED GPU ALIASES					
75 MEM_B_ODT<2..3> == NC_MEM_B_ODT<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		68 PM_EN_REG_GPU_CORE_S0 == NC_PM_EN_REG_GPU_CORE_S0 MAKE_BASE=TRUE NO_TEST=TRUE					
PCH GPIO		68 PM_PGOOD_REG_GPU_CORE_S0 == NC_PM_PGOOD_REG_GPU_CORE_S0 MAKE_BASE=TRUE NO_TEST=TRUE					
11 TP_PCH_GPIO64_CLKOUTFLEX0 == NC_PCH_GPIO64_CLKOUTFLEX0 MAKE_BASE=TRUE NO_TEST=TRUE		68 PM_EN_REG_GPU_VDDQ_S0 == NC_PM_EN_REG_GPU_VDDQ_S0 MAKE_BASE=TRUE NO_TEST=TRUE					
11 TP_PCH_GPIO65_CLKOUTFLEX1 == NC_PCH_GPIO65_CLKOUTFLEX1 MAKE_BASE=TRUE NO_TEST=TRUE		68 PM_PGOOD_REG_GPU_VDDQ_S0 == NC_PM_PGOOD_REG_GPU_VDDQ_S0 MAKE_BASE=TRUE NO_TEST=TRUE					
11 TP_PCH_GPIO66_CLKOUTFLEX2 == NC_PCH_GPIO66_CLKOUTFLEX2 MAKE_BASE=TRUE NO_TEST=TRUE		UNUSED PEG ALIASES					
11 TP_PCH_GPIO67_CLKOUTFLEX3 == NC_PCH_GPIO67_CLKOUTFLEX3 MAKE_BASE=TRUE NO_TEST=TRUE		5 =PEG_D2R_P<0..15> == NC_PEG_D2R_P<0..15> MAKE_BASE=TRUE NO_TEST=TRUE					
UNUSED IG DISPLAY		5 =PEG_D2R_N<0..15> == NC_PEG_D2R_N<0..15> MAKE_BASE=TRUE NO_TEST=TRUE					
5 TP_DP_IG_A_MLP<3..0> == NC_DP_IG_A_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE		5 =PEG_R2D_C_P<0..15> == NC_PEG_R2D_C_P<0..15> MAKE_BASE=TRUE NO_TEST=TRUE					
5 TP_DP_IG_A_MLN<3..0> == NC_DP_IG_A_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE		5 =PEG_R2D_C_N<0..15> == NC_PEG_R2D_C_N<0..15> MAKE_BASE=TRUE NO_TEST=TRUE					
5 TP_DP_IG_A_AUXCHP == NC_DP_IG_A_AUXCHP MAKE_BASE=TRUE NO_TEST=TRUE		PCH PCI					
5 TP_DP_IG_A_AUXCHN == NC_DP_IG_A_AUXCHN MAKE_BASE=TRUE NO_TEST=TRUE		13 TP_LPC_DREQ0_L == NC_LPC_DREQ0_L MAKE_BASE=TRUE NO_TEST=TRUE					
PCH Miscellaneous							
11 TP_HDA_SDIN1 == NC_HDA_SDIN1 MAKE_BASE=TRUE NO_TEST=TRUE							
11 TP_HDA_SDIN2 == NC_HDA_SDIN2 MAKE_BASE=TRUE NO_TEST=TRUE							
11 TP_HDA_SDIN3 == NC_HDA_SDIN3 MAKE_BASE=TRUE NO_TEST=TRUE							
11 TP_PCI_CLK33M_OUT2 == NC_PCI_CLK33M_OUT2 MAKE_BASE=TRUE NO_TEST=TRUE							
11 TP_PCI_CLK33M_OUT3 == NC_PCI_CLK33M_OUT3 MAKE_BASE=TRUE NO_TEST=TRUE							
8	7	6	5	4	3	2	1

8		7		6		5		4		3		2		1	
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Functional / ICT Test															
Apple Inc.															
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J16 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, BOTTOM	NO_TYPE, BGA	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	=50_OHM_SE	12.7 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	*	Y	0.215 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	TOP,BOTTOM	Y	0.215 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	*	Y	0.170 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	*	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	0.138 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.138 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.110 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	Y	0.180 MM	0.085 MM	=STANDARD	0.140 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.180 MM	0.085 MM	=STANDARD	0.140 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.135 MM	0.085 MM	=STANDARD	0.160 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD	0.160 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.089 MM	0.085 MM	=STANDARD	0.220 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.085 MM	=STANDARD	0.220 MM	0.1 MM

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	*	0.076 MM	?
1X_DIELECTRIC	TOP,BOTTOM	0.071 MM	?

BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1000

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

Board Stack-up

Finished board thickness: 1.58 mm

Layer	Material	Thickness
Top	Signal	0.5 oz (Cu plated)
	Prepreg	0.071 mm
2	Plane	1 oz
	Prepreg	0.076 mm
3	Signal	0.5 oz
	Prepreg	0.435 mm
4	Plane	1 oz
	Core	0.127 mm
5	Plane	1 oz
	Prepreg	0.435 mm
6	Signal	0.5 oz
	Prepreg	0.076 mm
2	Plane	1 oz
	Prepreg	0.071 mm
Btm	Signal	0.5 oz (Cu plated)

DDR3

DDR3-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_34S	*	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=STANDARD	=STANDARD
DDR_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
DDR_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
DDR_42S_D	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	0.1016 MM	0.1016 MM
DDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
DDR_68D	*	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF
DDR_COMP	*	Y	0.305 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

Minimum diff spacing is 4 mil
Table 4-5, Intel Doc# 486712

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
POWER_DDR_P4MM	*	Y	0.400 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_DDR	*	POWER_DDR_P4MM
DDR_CLK_PHY	*	DDR_68D
DDR_CTRL_PHY	*	DDR_39S
DDR_CMD_PHY	*	DDR_34S
DDR_DQ_PHY	*	DDR_42S
DDR_DSOS_PHY	*	DDR_42S_D
DDR_COMP_PHY	*	DDR_COMP

DDR3 Power-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_DDR	*	=2:1_SPACING	?

DDR3-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DDR_CLK_ISO	*	=5:1_SPACING	?
DDR_CTRL_ISO	*	=3.5:1_SPACING	?
DDR_CTRL2CTRL	*	=2.5:1_SPACING	?
DDR_CMD_ISO	*	=3.5:1_SPACING	?
DDR_CMD2CMD	*	=2:1_SPACING	?
DDR_DATA_ISO	*	=3:1_SPACING	?
DDR_DQ2DQ	*	=2:1_SPACING	900
DDR_DQ2DQS	*	=3:1_SPACING	?
DDR_BL2BL	*	=3:1_SPACING	?
DDR_CH2CH	*	=6.5:1_SPACING	?
DDR_COMP_ISO	*	0.381 MM	?

Main Segment Min Spacing Rules (mils) (Shark Bay PDG, Intel Doc# 486712)

Table	Trace	Design	Iso	Design	Comments
4-2	4	(diff)	15	19.69	CLK trace spacing controlled by #68_OHM_DIFF
4-3	8	9.84	12	13.78	
4-4	6	7.87	12	13.78	
4-5	8.5	7.87	12	11.81	DQ or DQS to other signals not in the same bytelane (but not ch)
					DQ to DQ in the same bytelane of the same channel
			10	11.81	DQ to DQS in the same bytelane of the same channel
			12	11.81	DQ or DQS in different bytelanes of the same channel
			25	25.59	DQ or DQS in different channels
			-	25.59	DDR3 to any other signal not DDR3

Constraints

Clocks: CK[3:0], CK#[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CLK	*	*	DDR_CLK_ISO

Control: CS#[3:0], CKE[3:0], ODT[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CTRL	*	*	DDR_CTRL_ISO
DDR_CTRL	DDR_CTRL	*	DDR_CTRL2CTRL

Command: MA[15:0], RAS#, CAS#, WE# BS[2:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CMD	*	*	DDR_CMD_ISO
DDR_CMD	DDR_CMD	*	DDR_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_COMP	*	*	DDR_COMP_ISO

Data: DQS[7:0], DQS#[7:0], DQ[63:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_A_DQ_BYTE*	*	*	DDR_DATA_ISO
DDR_A_DQS*	*	*	DDR_DATA_ISO
DDR_B_DQ_BYTE*	*	*	DDR_DATA_ISO
DDR_B_DQS*	*	*	DDR_DATA_ISO
DDR_*_DQ_BYTE*	=SAME	*	DDR_DQ2DQ
DDR_A_DQ_BYTE*	DDR_A_DQS*	*	DDR_DQ2DQS
DDR_A_DQ_BYTE*	DDR_A_DQ_BYTE*	*	DDR_BL2BL
DDR_B_DQ_BYTE*	DDR_B_DQS*	*	DDR_DQ2DQS
DDR_B_DQ_BYTE*	DDR_B_DQ_BYTE*	*	DDR_DQ2BL
DDR_A_*	DDR_B_*	*	DDR_CH2CH

Note (1):

Deliberately set DQ to DQS spacing to 3:1 to avoid adding complexity to constraints, even though it can be less. Only one rule per channel is needed by trading off a little space.

Note (2):


Intel suggests 25 mil (0.65 mm) spacing for via to channel, and via to pad to two different channels. DDR3 draws about 20 mA per trace with edge rates in the 100s of ps. The main coupling mechanism is capacitive. A 0.65 mm spacing is used for power nets, which draw far more current (inductive coupling however). These rules are far too conservative. To meet these rules, the spacing must be applied to the net.

Note (3):

In order for the constraints $DDR_*_DQ_BYTE*$ to =SAME to win out over $DDR\{A,B\}_DQ_BYTE*$ to $DDR\{A,B\}_DQ_BYTE*$ so that the small intra-bytelane spacing is used, the spacing rule DDR_DQ2DQ must have a weight greater than DDR_BL2BL .

DDR3

Electrical Constraint Set	Physical	Spacing	
Channel A			
1890D DNR_A_CLK0	DNR_CLK_PHY	DNR_CLK	MEM A_CLK P<1...0>
1890D DNR_A_CLK0	DNR_CLK_PHY	DNR_CLK	MEM A_CLK N<1...0>
1890D DNR_A_CLK1	DNR_CLK_PHY	DNR_CLK	MEM A_CLK P<3...2>
1890D DNR_A_CLK1	DNR_CLK_PHY	DNR_CLK	MEM A_CLK N<3...2>
1890D DNR_A_CTL0	DNR_CTL_PHY	DNR_CTL	MEM A_CKE<1...0>
1890D DNR_A_CTL0	DNR_CTL_PHY	DNR_CTL	MEM A_CS L<1...0>
1890D DNR_A_CTL0	DNR_CTL_PHY	DNR_CTL	MEM A_ODT<1...0>
1890D DNR_A_CTL1	DNR_CTL_PHY	DNR_CTL	MEM A_CKE<3...2>
1890D DNR_A_CTL1	DNR_CTL_PHY	DNR_CTL	MEM A_CS L<3...2>
1890D DNR_A_CTL1	DNR_CTL_PHY	DNR_CTL	MEM A_ODT<3...2>
1890D DNR_A_CMD	DNR_CMD_PHY	DNR_CMD	MEM A_A<15...0>
1890D DNR_A_CMD	DNR_CMD_PHY	DNR_CMD	MEM A_BA<2...0>
1890D DNR_A_CMD	DNR_CMD_PHY	DNR_CMD	MEM A_RAS_L
1890D DNR_A_CMD	DNR_CMD_PHY	DNR_CMD	MEM A_CAS_L
1890D DNR_A_CMD	DNR_CMD_PHY	DNR_CMD	MEM A_WE_L
1890D DNR_A_DQ_BVTE0	DNR_DQ_PHY	DNR_A_DQ_BVTE0	MEM A_DQ<7...0>
1890D DNR_A_DQ_BVTE1	DNR_DQ_PHY	DNR_A_DQ_BVTE1	MEM A_DQ<15...8>
1890D DNR_A_DQ_BVTE2	DNR_DQ_PHY	DNR_A_DQ_BVTE2	MEM A_DQ<23...16>
1890D DNR_A_DQ_BVTE3	DNR_DQ_PHY	DNR_A_DQ_BVTE3	MEM A_DQ<31...24>
1890D DNR_A_DQ_BVTE4	DNR_DQ_PHY	DNR_A_DQ_BVTE4	MEM A_DQ<39...32>
1890D DNR_A_DQ_BVTE5	DNR_DQ_PHY	DNR_A_DQ_BVTE5	MEM A_DQ<47...40>
1890D DNR_A_DQ_BVTE6	DNR_DQ_PHY	DNR_A_DQ_BVTE6	MEM A_DQ<55...48>
1890D DNR_A_DQ_BVTE7	DNR_DQ_PHY	DNR_A_DQ_BVTE7	MEM A_DQ<63...56>
1890D DNR_A_DQS0	DNR_DQS_PHY	DNR_A_DQS0	MEM A_DQS P<0>
1890D DNR_A_DQS0	DNR_DQS_PHY	DNR_A_DQS0	MEM A_DQS N<0>
1890D DNR_A_DQS1	DNR_DQS_PHY	DNR_A_DQS1	MEM A_DQS P<1>
1890D DNR_A_DQS1	DNR_DQS_PHY	DNR_A_DQS1	MEM A_DQS N<1>
1890D DNR_A_DQS2	DNR_DQS_PHY	DNR_A_DQS2	MEM A_DQS P<2>
1890D DNR_A_DQS2	DNR_DQS_PHY	DNR_A_DQS2	MEM A_DQS N<2>
1890D DNR_A_DQS3	DNR_DQS_PHY	DNR_A_DQS3	MEM A_DQS P<3>
1890D DNR_A_DQS3	DNR_DQS_PHY	DNR_A_DQS3	MEM A_DQS N<3>
1890D DNR_A_DQS4	DNR_DQS_PHY	DNR_A_DQS4	MEM A_DQS P<4>
1890D DNR_A_DQS4	DNR_DQS_PHY	DNR_A_DQS4	MEM A_DQS N<4>
1890D DNR_A_DQS5	DNR_DQS_PHY	DNR_A_DQS5	MEM A_DQS P<5>
1890D DNR_A_DQS5	DNR_DQS_PHY	DNR_A_DQS5	MEM A_DQS N<5>
1890D DNR_A_DQS6	DNR_DQS_PHY	DNR_A_DQS6	MEM A_DQS P<6>
1890D DNR_A_DQS6	DNR_DQS_PHY	DNR_A_DQS6	MEM A_DQS N<6>
1890D DNR_A_DQS7	DNR_DQS_PHY	DNR_A_DQS7	MEM A_DQS P<7>
1890D DNR_A_DQS7	DNR_DQS_PHY	DNR_A_DQS7	MEM A_DQS N<7>
Channel B			
1890D DNR_B_CLK0	DNR_CLK_PHY	DNR_CLK	MEM B_CLK P<1...0>
1890D DNR_B_CLK0	DNR_CLK_PHY	DNR_CLK	MEM B_CLK N<1...0>
1890D DNR_B_CLK1	DNR_CLK_PHY	DNR_CLK	MEM B_CLK P<3...2>
1890D DNR_B_CLK1	DNR_CLK_PHY	DNR_CLK	MEM B_CLK N<3...2>
1890D DNR_B_CTL0	DNR_CTL_PHY	DNR_CTL	MEM B_CKE<1...0>
1890D DNR_B_CTL0	DNR_CTL_PHY	DNR_CTL	MEM B_CS L<1...0>
1890D DNR_B_CTL0	DNR_CTL_PHY	DNR_CTL	MEM B_ODT<1...0>
1890D DNR_B_CTL1	DNR_CTL_PHY	DNR_CTL	MEM B_CKE<3...2>
1890D DNR_B_CTL1	DNR_CTL_PHY	DNR_CTL	MEM B_CS L<3...2>
1890D DNR_B_CTL1	DNR_CTL_PHY	DNR_CTL	MEM B_ODT<3...2>
1890D DNR_B_CMD	DNR_CMD_PHY	DNR_CMD	MEM B_A<15...0>
1890D DNR_B_CMD	DNR_CMD_PHY	DNR_CMD	MEM B_BA<2...0>
1890D DNR_B_CMD	DNR_CMD_PHY	DNR_CMD	MEM B_RAS_L
1890D DNR_B_CMD	DNR_CMD_PHY	DNR_CMD	MEM B_CAS_L
1890D DNR_B_CMD	DNR_CMD_PHY	DNR_CMD	MEM B_WE_L
1890D DNR_B_DQ_BVTE0	DNR_DQ_PHY	DNR_B_DQ_BVTE0	MEM B_DQ<7...0>
1890D DNR_B_DQ_BVTE1	DNR_DQ_PHY	DNR_B_DQ_BVTE1	MEM B_DQ<15...8>
1890D DNR_B_DQ_BVTE2	DNR_DQ_PHY	DNR_B_DQ_BVTE2	MEM B_DQ<23...16>
1890D DNR_B_DQ_BVTE3	DNR_DQ_PHY	DNR_B_DQ_BVTE3	MEM B_DQ<31...24>
1890D DNR_B_DQ_BVTE4	DNR_DQ_PHY	DNR_B_DQ_BVTE4	MEM B_DQ<39...32>
1890D DNR_B_DQ_BVTE5	DNR_DQ_PHY	DNR_B_DQ_BVTE5	MEM B_DQ<47...40>
1890D DNR_B_DQ_BVTE6	DNR_DQ_PHY	DNR_B_DQ_BVTE6	MEM B_DQ<55...48>
1890D DNR_B_DQ_BVTE7	DNR_DQ_PHY	DNR_B_DQ_BVTE7	MEM B_DQ<63...56>
1890D DNR_B_DQS0	DNR_DQS_PHY	DNR_B_DQS0	MEM B_DQS P<0>
1890D DNR_B_DQS0	DNR_DQS_PHY	DNR_B_DQS0	MEM B_DQS N<0>
1890D DNR_B_DQS1	DNR_DQS_PHY	DNR_B_DQS1	MEM B_DQS P<1>
1890D DNR_B_DQS1	DNR_DQS_PHY	DNR_B_DQS1	MEM B_DQS N<1>
1890D DNR_B_DQS2	DNR_DQS_PHY	DNR_B_DQS2	MEM B_DQS P<2>
1890D DNR_B_DQS2	DNR_DQS_PHY	DNR_B_DQS2	MEM B_DQS N<2>
1890D DNR_B_DQS3	DNR_DQS_PHY	DNR_B_DQS3	MEM B_DQS P<3>
1890D DNR_B_DQS3	DNR_DQS_PHY	DNR_B_DQS3	MEM B_DQS N<3>
1890D DNR_B_DQS4	DNR_DQS_PHY	DNR_B_DQS4	MEM B_DQS P<4>
1890D DNR_B_DQS4	DNR_DQS_PHY	DNR_B_DQS4	MEM B_DQS N<4>
1890D DNR_B_DQS5	DNR_DQS_PHY	DNR_B_DQS5	MEM B_DQS P<5>
1890D DNR_B_DQS5	DNR_DQS_PHY	DNR_B_DQS5	MEM B_DQS N<5>
1890D DNR_B_DQS6	DNR_DQS_PHY	DNR_B_DQS6	MEM B_DQS P<6>
1890D DNR_B_DQS6	DNR_DQS_PHY	DNR_B_DQS6	MEM B_DQS N<6>
1890D DNR_B_DQS7	DNR_DQS_PHY	DNR_B_DQS7	MEM B_DQS P<7>
1890D DNR_B_DQS7	DNR_DQS_PHY	DNR_B_DQS7	MEM B_DQS N<7>
Reset			
1890D	DNR_S08		MEM RESET_L
SM COMP			
1890D	DNR_COMP_PHY	DNR_COMP	CPU_SM_RCOMP<0...2>

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PCI Express/DMI

PCIe-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
PCIE_COMP	*	Y	0.305 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_PCIE_PHY	*	PCIE_90D
COMP_PCIE_PHY	*	PCIE_COMP
CPU_ASYNC_PHY	*	CPU_50S

PCIE and DMI Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
4-5	50	50	15	15.75	PCIE. Impedance inferred from Table 4-7.
4-7	50	50	8	15.75	DMI. Numbers based on Intel stack-up.

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_ISO	*	=5:1_SPACING	?
COMP_PCIE_ISO	*	=4:1_SPACING	?
CPU_ASYNC_ISO	*	=3:1_SPACING	?
CPU_MS_ISO	TOP,BOTTOM	=4.5:1_SPACING	?
CPU_MS_ISO	*	=3:1_SPACING	?

Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	*	*	CLK_PCIE_ISO
COMP_PCIE	*	*	COMP_PCIE_ISO
CPU_ASYNC	*	*	CPU_ASYNC_ISO
CPU_ASYNC_MS	*	*	CPU_MS_ISO

PEG Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
4.2.1	80	80	16	15.75	PCIe Gen3. Allow looser spacing for same direction on stripline per Anil

CPU ASYNCHRONOUS

Electrical Constraint Set	Physical	Spacing	
REMARK	CPU_ASYNC_PHY	CPU_ASYNC	CPU_PROCHOT_L 6 44 45 61 62
REMARK	CPU_ASYNC_PHY	CPU_ASYNC	CPU_PROCHOT_R_L 6
REMARK PECTI	CPU_ASYNC_PHY	CPU_ASYNC_MS	CPU_PECTI 6 14 44 45
REMARK	CPU_ASYNC_PHY	CPU_ASYNC_MS	SMC_PECTI_L 44 45
REMARK	CPU_ASYNC_PHY	CPU_ASYNC	CPU_CATERER_L 6 45
REMARK	CPU_ASYNC_PHY	CPU_ASYNC	CPU_PWRGD 6 14 18
REMARK	CPU_ASYNC_PHY	CPU_ASYNC	PM_SYNC 6 12
REMARK	CPU_ASYNC_PHY	CPU_ASYNC	PM_THRMTRIP_L 6 14 45
REMARK	CPU_ASYNC_PHY	CPU_ASYNC	CPU_RESET_L 6 14 18
REMARK XDP_BPM_L	CPU_ASYNC_PHY	CPU_ASYNC	XDP_BPM_L<1..0> 6 18

PCIe (CPU)

Electrical Constraint Set	Physical	Spacing	
CPU PCIe Compensation	COMP_PCIE_PHY	COMP_PCIE	CPU_PEG_RCOMP
CPU eDP Compensation	COMP_PCIE_PHY	COMP_PCIE	CPU_EDP_RCOMP
	COMP_PCIE_PHY	COMP_PCIE	CPU_CFG_RCOMP

Physical Net Type to Rule Map		
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_PHY	*	PCIE_85D
COMP_DMI_PHY	*	DMI_COMP

PCie-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_SAME_DIR	*	=3.5X_DIELECTRIC	?
PCIE_ALT_DIR	*	=7X_DIELECTRIC	?
PCIE_ISO	*	=4:1_SPACING	?

TBT x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_TBT_R2D	PCIE_TBT_R2D	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_D2R	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_R2D	*	PCIE_ALT_DIR
PCIE_TBT_D2R	*	*	PCIE_ISO
PCIE_TBT_R2D	*	*	PCIE_ISO

PCH x1 PCIE Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	PCIE_ISO

DMI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
DMI_SAME_DIR	*	=4X_DIELECTRIC	?
DMI_ALT_DIR	*	=5X_DIELECTRIC	?
DMI_ISO	*	=4X_DIELECTRIC	?

DMI x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_N2S	DMI_N2S	*	DMI_SAME_DIR
DMI_S2N	DMI_S2N	*	DMI_SAME_DIR
DMI_N2S	DMI_S2N	*	DMI_ALT_DIR
DMI_N2S	*	*	DMI_ISO
DMI_S2N	*	*	DMI_ISO

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DMI_COMP	*	Y	0.2032 MM	0.2032 MM	3 MM	=STANDARD	=STANDARD

PCie (PCH)


Electrical Constraint Set	Physical	Spacing
x4 Thunderbolt		
PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D
PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D
PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D
PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D
PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R
PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R
PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R
PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE
x1 AirPort		
PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE
PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE
PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE
PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE
PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE
PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE
x1 Caesar IV		
PCIE_GEN2_R2D	PCIE_PHY	PCIE
PCIE_GEN2_R2D	PCIE_PHY	PCIE
PCIE_GEN2_R2D	PCIE_PHY	PCIE
PCIE_GEN2_R2D	PCIE_PHY	PCIE
PCIE_GEN2_D2R	PCIE_PHY	PCIE
PCIE_GEN2_D2R	PCIE_PHY	PCIE
PCIE_GEN2_D2R	PCIE_PHY	PCIE
PCIE_GEN2_D2R	PCIE_PHY	PCIE
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE
x2 SSD		
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE
PCH PCIE Compensation		
COMP_DMI_PHY	COMP_PCIE	PCH_PCIE_RCOMP

CPU DP REF CLK

Electrical Constraint Set	Physical	Spacing
CPU DP REF CLK		
CPU_CLK135_DLL	PCIE_PHY	CLK_PCIE
CPU_CLK135_DLL	PCIE_PHY	CLK_PCIE
CPU_CLK135_DLL	PCIE_PHY	CLK_PCIE
CPU_CLK135_DLL	PCIE_PHY	CLK_PCIE

DMI

Electrical Constraint Set	Physical	Spacing
DMI		
DMI_N2S	PCIE_PHY	DMI_N2S
DMI_N2S	PCIE_PHY	DMI_N2S
DMI_S2N	PCIE_PHY	DMI_S2N
DMI_S2N	PCIE_PHY	DMI_S2N
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE
DMI Compensation		
COMP_DMI_PHY	COMP_PCIE	PCH_DMI_RCOMP

C MASTER=J16 NICK		SYNC DATE=01/10/2013	
PCH PCIe/DMI Constraints			
 Apple Inc.	DRAWING NUMBER		8126
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	12.4.0		
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PCH

PCH-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCH-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	=4:1_SPACING	?
COMP_PCH	*	=2:1_SPACING	?

PCI

PCI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCI	*	=2:1_SPACING	?

LPC

LPC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

LPC-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5:1_SPACING	?
CLK_LPC	*	=2:1_SPACING	?

HDA

HDA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

HDA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

Crystal

Crystal-specific Physical Rules

[illegible]

Crystal-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

SPI

SPI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=2:1_SPACING	?

PCI

Electrode

Electrical Constraint Set	Physical	Spacing	
PCI Clock			
	CLK_PCT_55S	CLK_PCT	PCH_CLK33M_PCIEIN 11 19
	CLK_PCT_55S	CLK_PCT	PCH_CLK33M_PCIEOUT 11 19

LPC

[illegible]

Electrical Constraint Set	Physical	Spacing	
LPC			
ES35	LPC_55S	LPC	LPC AD<3..0> 13 44
ES36	LPC_55S	LPC	LPC AD R<3..0> 13
ES37	LPC_55S	LPC	LPC FRAME_L 13 44
ES38	LPC_55S	LPC	LPC FRAME_R_L 13 44
LPC Clocks			
ES39	CLK LPC_55S	CLK LPC	LPC CLK33M LPCPLUS 13 44
ES40	CLK LPC_55S	CLK LPC	LPC CLK33M LPCPLUS_R 13 19
ES41	CLK LPC_55S	CLK LPC	LPC CLK33M SMC 19 44
ES42	CLK LPC_55S	CLK LPC	LPC CLK33M SMC_R 13 19

PCH Clocks

Estimate of the effect of the intervention on the outcome	Estimate of the effect of the intervention on the outcome	Estimate of the effect of the intervention on the outcome
...

Electrical Constraint Set	Physical	Spacing	
PCH Reference Clock			
PC100	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_SB 11 19
PC100	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_SB_R 11
PCH RTC 32K			
PC100	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1 11 19
PC100	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2 11 19
PC100	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2_R 19
SMC 32K			
PC100	CLK_PCH_55S	CLK_PCH	PM_CLK32K_SUSCLK_R 12 45
PC100	CLK_PCH_55S	CLK_PCH	SMC_CLK32K 44 45













25 MHz Reference Clocks

Elemental	Quantitative	Elemental	Quantitative
...

Electrical Constraint Set	Physical	Spacing		
25M Reference Crystal				
REF	CLK_XTAL	XTAL	SYSCLK_CLK25M_X1	19
REF	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2	19
REF	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2_R	19
25M Reference Clocks				
REF	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_ENET	19 35
REF	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_ENET_R	19
REF	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_TBT	19 26
REF	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_TBT_R	26

HDA

Plants used

Electrical Constraint Set	Physical	Spacing		
HDA				
	HDA_55S	HDA	HDA_BIT_CLK	11 52
	HDA_55S	HDA	HDA_BIT_CLK_R	11 53
	HDA_55S	HDA	HDA_RST_L	11 54
	HDA_55S	HDA	HDA_RST_R_L	11 55
	HDA_55S	HDA	HDA_SPOUT	11 56
	HDA_55S	HDA	HDA_SPOUT_R	11 57
	HDA_55S	HDA	HDA_SYNC	11 58
	HDA_55S	HDA	HDA_SYNC_R	11 59
	HDA_55S	HDA	HDA_SDIO	11 60
	HDA_55S	HDA	AUD_SDI_R	52
SPDIF				
		HDA	AUD_SPDIF_CHIP	52
		HDA	AUD_SPDIF_OUT	52 56

SPI Bootrom

Electrical	Constraint	Cost	Physical	Capacity
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Electrical Constraint Set		Physical	Spacing	
SPI ROM				
R997		SPI_50S	SPT	SPI_CLK_R 13 46
R997		SPT_50S	SPT	SPI_CLK 46
R998		SPI_50S	SPT	SPI_ALT_CLK 46
R998		SPT_50S	SPT	SPI_SMC_CLK 44 46
R999		SPT_50S	SPT	SPI_MLB_CLK 46
R999		SPI_50S	SPT	SPI_CS0_R_L 13 46
R999		SPT_50S	SPT	SPI_CS0_L 46
R999		SPT_50S	SPT	SPI_ALT_CS_L 46
R999		SPT_50S	SPT	SPI_SMC_CS_L 44 46
R999		SPT_50S	SPT	SPI_MLB_CS_L 46
R999		SPT_50S	SPT	SPI_MOSI_R 13 46
R999		SPT_50S	SPT	SPI_MOSI 46
R999		SPT_50S	SPT	SPI_ALT_MOSI 46
R999		SPT_50S	SPT	SPI_SMC_MOSI 44 46
R999		SPT_50S	SPT	SPI_MLB_MOSI 46
R999		SPT_50S	SPT	SPI_MISO 13 46
R999		SPT_50S	SPT	SPI_ALT_MISO 46
R999		SPT_50S	SPT	SPI_SMC_MISO 44 46
R999		SPT_50S	SPT	SPI_MLB_MISO 46
R999		SPT_50S	SPT	SPIROM_USE_MLB 14 46

D

C

B

A

Section	Imp	Design	Iso	Design	Comments
12.2.1	90	90	12	11.81	USB 2.0
13.3.1	85	85	20	21.65	USB 3.0

Section	Imp	Design	Iso	Design	Comments
12.2.1	90	90	12	11.81	USB 2.0
13.3.1	85	85	20	21.65	USB 3.0

Constraints Ethernet

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF

SD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SD	*	*	SD_ISO

x I/F (SMIA/MIPI)

MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

TWV

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMIA_DIFF	*	*	SMIA_DIFF_ISO
SMIA_DIFF	SMIA_DIFF	*	SMIA_DIFF2DIFF

	6
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[illegible]

External Port C (J4700)				
REF0	USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_P 43
REF0	USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_N 43
REF0		USB3_PHY	USB3	USB3_EXTC_RX_F_P 13 43
REF0		USB3_PHY	USB3	USB3_EXTC_RX_F_N 13 43
REF0	USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_P 13 43
REF0	USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_N 13 43
REF0		USB3_PHY	USB3	USB3_EXTC_TX_F_P 43
REF0		USB3_PHY	USB3	USB3_EXTC_TX_F_N 43
REF0		USB3_PHY	USB3	USB3_EXTC_TX_C_P 43
REF0		USB3_PHY	USB3	USB3_EXTC_TX_C_N 43
REF0	USB2_CONN	USB2_PHY	USB2	USB_EXTC_1_P 13 43
REF0	USB2_CONN	USB2_PHY	USB2	USB_EXTC_1_N 13 43
REF0		USB2_PHY	USB2	USB2_EXTC_P 43
REF0		USB2_PHY	USB2	USB2_EXTC_N 43





External Port D (J4710)					
RE50	USB1_RX_CONN	USB1_PHY	USB1	USB1_EXTD_RX_P	43
RE50	USB1_RX_CONN	USB1_PHY	USB1	USB1_EXTD_RX_N	43
RE50	USB1_RX_CONN	USB1_PHY	USB1	USB1_EXTD_RX_F_P	13 43
RE50	USB1_RX_CONN	USB1_PHY	USB1	USB1_EXTD_RX_F_N	13 43
RE50	USB1_TX_CONN	USB1_PHY	USB1	USB1_EXTD_TX_P	13 43
RE50	USB1_TX_CONN	USB1_PHY	USB1	USB1_EXTD_TX_N	13 43
RE50	USB1_TX_CONN	USB1_PHY	USB1	USB1_EXTD_TX_F_P	43
RE50	USB1_TX_CONN	USB1_PHY	USB1	USB1_EXTD_TX_F_N	43
RE50	USB1_TX_CONN	USB1_PHY	USB1	USB1_EXTD_TX_C_P	43
RE50	USB1_TX_CONN	USB1_PHY	USB1	USB1_EXTD_TX_C_N	43
RE50	USB2_CONN	USB2_PHY	USB2	USB_EXTD_9_P	13 43
RE50	USB2_CONN	USB2_PHY	USB2	USB_EXTD_9_N	13 43
RE50		USB2_PHY	USB2	USB2_EXTD_P	43
RE50		USB2_PHY	USB2	USB2_EXTD_N	43
Camera (J73510)					
RE50	USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_P	13 38
				USB_CAMERA_N	

PCH USB Compensation	PCH_55S	COMP_PCH	PCH_USB_BIAS	13
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Et tu Brute?

Electrical Constraint Set		Physical	Spacing		
Ethernet					
ENET	ENET_MDI	ENET_DIFF_PHV	ENET_DIFF	ENETCONN MDI P<3..0>	15 36
ENET	ENET_MDI	ENET_DIFF_PHV	ENET_DIFF	ENETCONN MDI N<3..0>	15 36
ENET		ENET_DIFF_PHV	ENET_TRANS	ENETCONN MDI T P<3..0>	15 36
ENET		ENET_DIFF_PHV	ENET_TRANS	ENETCONN MDI T N<3..0>	15 36
ENET			ENET_TRANS	ENETCONN MCT0	15 36
ENET			ENET_TRANS	ENETCONN MCT1	15 36
ENET			ENET_TRANS	ENETCONN MCT2	15 36
ENET			ENET_TRANS	ENETCONN MCT3	15 36
ENET			ENET_TRANS	ENETCONN MCT BS	15 36
ENET		ENET_COMP_PHV	COMP_ENET	ENET_RDAC	15
SD					
SD	SD_DATA	SD_PHV	SD	ENET_CR_DATA<7..0>	15 36
SD		SD_PHV	SD	SDCONN_DATA<7..0>	15 36


ENET		SD_PHY	SD	SDCONN_DETECT_L	35
ENET	SD_CMD	SD_PHY	SD	ENET_SD_CMD	36
ENET		SD_PHY	SD	SDCONN_CMD	35
ENET		SD_PHY	SD	SDCONN_CMD_R	37
ENET	SD_CLK	SD_PHY	SD	ENET_SD_CLK	36
ENET		SD_PHY	SD	SDCONN_CLK	36
ENET		SD_PHY	SD	SDCONN_CLK_R	37
ENET		SD_PHY	SD	ENET_MEDIA_SENSE	11
ENET		SD_PHY	SD	ENET_SD_DETECT_L	35

CIV SPI				
	CIV_SPI	SPI	ENET_SCLK	35
	CIV_SPI	SPI	ENET_MISO	35
	CIV_SPI	SPI	ENET_MOSI	35
	CIV_SPI	SPI	ENET_CS_L	35

SYNCH MASTER-T16.MIR SYNCH DATE=12/03/2013 A

SYNC MASTER=J16 MLB PAGE TITLE USB/Ethernet/SD Constrai		SYNC DATE=12/	
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SYNC MASTER=J16 MLB		SYNC DATE=12/03/2012	
PAGE TITLE			
USB/Ethernet/SD Constraints			
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DC-DC

Power-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GND_P3MM	*	Y	0.300 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
GND_P5MM	*	Y	0.500 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
POWER_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
POWER_P3MM	*	Y	0.300 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
POWER_P6MM	*	Y	0.600 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND	*	GND_P5MM
GND	BGA	GND_P3MM
POWER	*	POWER_P6MM
POWER	BGA	POWER_P3MM
VR_CTL_PHY	*	POWER_P3MM
VR_CTL_PHY	BGA	STANDARD
VR_VID_PHY	*	POWER_50S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VR_DIDT_PHY	*	POWER_P6MM
VR_DIDT_PHY	BGA	STANDARD

Power-specific Spacing Definitions

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_ISO	*	=STANDARD	?
GND_ISO	*	=STANDARD	?

Constraints
Power and Common

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	POWER_ISO
GND	*	*	GND_ISO

DC-DC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SWNODE_ISO	*	=8:1_SPACING	1000
SWNODE_SW2SW	*	=1:1_SPACING	?
SWNODE_SW2PWR	*	=2:1_SPACING	?
SWNODE_SW2GND	*	=2:1_SPACING	?

DC-DC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_SWITCH	*	*	SWNODE_ISO
VR_SWITCH	*	BGA	BGA_P1MM
VR_SWITCH	VR_SWITCH	*	SWNODE_SW2SW
VR_SWITCH	POWER	*	SWNODE_SW2PWR
VR_SWITCH	GND	*	SWNODE_SW2GND

DC-DC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_ISO	*	=3:1_SPACING	?
VR_VID_ISO	*	=4X_DIELECTRIC	?

DC-DC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CTL	*	*	VR_CTL_ISO
VR_VID	*	*	VR_VID_ISO

VDDQ S3 (1.35V)/VTT S0

Physical	Spacing	Voltage	D1D2	NO_TEST	
Input Bus					
FE4 POWER	POWER	5V			REG_V5IN_U7300
Local Ground					
FE4 GND	GND	0V			AGND_VDDQ3
VDDQ S3					
FE4 VR_D1D2_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQ3
FE4 VR_D1D2_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQ3_L
FE4 VR_D1D2_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VDDQ3
FE4 VR_D1D2_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VDDQ3_RC
FE4 VR_D1D2_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQ3
FE4 VR_D1D2_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQ3_R
FE4 VR_D1D2_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_VDDQ3
FE4 VR_D1D2_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_VDDQ3
FE4 VR_CTL_PHY	VR_CTL				REG_VDDQ3_VDDQNS
FE4 VR_CTL_PHY	VR_CTL				REG_VDDQ3_VREF
FE4 VR_CTL_PHY	VR_CTL				REG_VDDQ3_REFIN
FE4 VR_CTL_PHY	VR_CTL				REG_VDDQ3_MODE
FE4 VR_CTL_PHY	VR_CTL				REG_VDDQ3_TRIP
FE4 VR_CTL_PHY	VR_CTL				LDO_DDEVRTT0_SNS
FE4 VR_CTL_PHY	VR_CTL				REG_VDDQ3_VTTREF
Output Bus					
FE4 POWER	POWER	1.35V			PPVDDQ_S3
FE4 POWER_DDR	POWER_DDR	0.675V			PPDDEVRTT_S0
FET Switched					
FE4 POWER	POWER	1.35V			PPVDDQ_S0
Sensed					
FE4 POWER	POWER	1.35V			PPVDDQ_S3_DDR
FE4 POWER	POWER	1.35V			PPVDDQ_S0_CPU

PCH/GPU/TBT 1.05V S0


Electrical Constraint Set	Physical	Spacing	Voltage	D1D2	NO_TEST
Input Bus					
REG	POWER	POWER	5V		REG VCC U7400
REG	POWER	POWER	5V		REG PVCC U7400
Local Ground					
REG	GND	GND	0V		AGND P1V05S0
1.05V S0					
REG	VR_D1D2_PHY	VR_SWITCH	12V	TRUE	REG PHASE P1V05S0
REG	VR_D1D2_PHY	VR_SWITCH	12V	TRUE	REG PHASE P1V05S0 L
REG	VR_D1D2_PHY	VR_SWITCH	12V	TRUE	REG BOOT P1V05S0
REG	VR_D1D2_PHY	VR_SWITCH	12V	TRUE	REG BOOT P1V05S0 RC
REG	VR_D1D2_PHY	VR_SWITCH	12V	TRUE	REG UGATE P1V05S0
REG	VR_D1D2_PHY	VR_SWITCH	12V	TRUE	REG UGATE P1V05S0 R
REG	VR_D1D2_PHY	VR_SWITCH	12V	TRUE	REG LGATE P1V05S0
REG	VR_D1D2_PHY	VR_SWITCH	12V	TRUE	REG SNUBBER P1V05S0
REG	VR_CTL_PHY	VR_CTL			REG P1V05S0 OCSET
REG	VR_CTL_PHY	VR_CTL			REG P1V05S0 VO
REG		SENSE			REG P1V05S0 FB
REG		SENSE			REG P1V05S0 RTN
REG	VR_CTL_PHY	VR_CTL			REG P1V05S0 SREF
REG	VR_CTL_PHY	VR_CTL			REG P1V05S0 FSEL
Output Bus					
REG	POWER	POWER	1.05V		PP1V05_S0
FET Switched					
REG	POWER	POWER	1.05V		PP1V05_TBTLIC
REG	POWER	POWER	1.05V		PP1V05_TBTCIO

8	7	6	5	4	3	2	1																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																														
CPU VCC Phases				CPU VCC Controller																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
<table><tr><th>Electrical Constraint Set</th><th>Physical</th><th>Spacing</th><th>Voltage</th><th>DIDT</th><th>NO_TEST</th></tr><tr><td colspan="6">Input Bus</td></tr><tr><td>1397</td><td>POWER</td><td>POWER</td><td>1.2V</td><td></td><td>PP12V_S0_CPUVCC FLT 61 62</td></tr><tr><td>1398</td><td>POWER</td><td>POWER</td><td>5V</td><td></td><td>REG_VCC_U7000 61</td></tr><tr><td colspan="6">Local Ground</td></tr><tr><td>1399</td><td>GND</td><td>GND</td><td>0V</td><td></td><td>AGND_CPU 61 62 71</td></tr><tr><td colspan="6">Phase 1</td></tr><tr><td>1400</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_THWN_1 62</td></tr><tr><td>1401</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_PWM_CPUVCC_1 61 62</td></tr><tr><td>1402</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_PWM_CPUVCC_1_R 61</td></tr><tr><td>1403</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td>REG_PHASE_CPUVCC_1 62</td></tr><tr><td>1404</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td>REG_PHASE_CPUVCC1 62</td></tr><tr><td>1405</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td>REG_BOOT_CPUVCC_1 62</td></tr><tr><td>1406</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td>REG_BOOT_CPUVCC_1_RC 62</td></tr><tr><td>1407</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td>REG_SNUBBER_CPUVCC_1 62</td></tr><tr><td>1408</td><td>POWER</td><td>POWER</td><td>1.8V</td><td></td><td>PPCPUVCC_S0_SENSE_1 62</td></tr><tr><td>1409</td><td>SNS_DIFF_PHY</td><td>SENSE</td><td></td><td></td><td>REG_ISENVCC_1_P 61 62</td></tr><tr><td>1410</td><td>SNS_DIFF_PHY</td><td>SENSE</td><td></td><td></td><td>REG_ISENVCC_1_N 62</td></tr><tr><td>1411</td><td>SNS_DIFF_PHY</td><td>SENSE</td><td></td><td></td><td>REG_ISENVCC_1_NR 61 62</td></tr><tr><td colspan="6">Phase 2</td></tr><tr><td>1412</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_THWN_2 62</td></tr><tr><td>1413</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_PWM_CPUVCC_2 61 62</td></tr><tr><td>1414</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_PWM_CPUVCC_2_R 61</td></tr><tr><td>1415</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td>REG_PHASE_CPUVCC_2 62</td></tr><tr><td>1416</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td>REG_PHASE_CPUVCC2 62</td></tr><tr><td>1417</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td>REG_BOOT_CPUVCC_2 62</td></tr><tr><td>1418</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td>REG_BOOT_CPUVCC_2_RC 62</td></tr><tr><td>1419</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td>REG_SNUBBER_CPUVCC_2 62</td></tr><tr><td>1420</td><td>POWER</td><td>POWER</td><td>1.8V</td><td></td><td>PPCPUVCC_S0_SENSE_2 62</td></tr><tr><td>1421</td><td>SNS_DIFF_PHY</td><td>SENSE</td><td></td><td></td><td>REG_ISENVCC_2_P 61 62</td></tr><tr><td>1422</td><td>SNS_DIFF_PHY</td><td>SENSE</td><td></td><td></td><td>REG_ISENVCC_2_N 62</td></tr><tr><td>1423</td><td>SNS_DIFF_PHY</td><td>SENSE</td><td></td><td></td><td>REG_ISENVCC_2_NR 61 62</td></tr><tr><td colspan="6">Phase 3</td></tr><tr><td>1424</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_THWN_3 62</td></tr><tr><td>1425</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_PWM_CPUVCC_3 61 62</td></tr><tr><td>1426</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_PWM_CPUVCC_3_R 61</td></tr><tr><td>1427</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td>REG_PHASE_CPUVCC_3 62</td></tr><tr><td>1428</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td>REG_PHASE_CPUVCC3 62</td></tr><tr><td>1429</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td>REG_BOOT_CPUVCC_3 62</td></tr><tr><td>1430</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td>REG_BOOT_CPUVCC_3_RC 62</td></tr><tr><td>1431</td><td>VR_CTL_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td>REG_SNUBBER_CPUVCC_3 62</td></tr><tr><td>1432</td><td>POWER</td><td>POWER</td><td>1.8V</td><td></td><td>PPCPUVCC_S0_SENSE_3 62</td></tr><tr><td>1433</td><td>SNS_DIFF_PHY</td><td>SENSE</td><td></td><td></td><td>REG_ISENVCC_3_P 61 62</td></tr><tr><td>1434</td><td>SNS_DIFF_PHY</td><td>SENSE</td><td></td><td></td><td>REG_ISENVCC_3_N 62</td></tr><tr><td>1435</td><td>SNS_DIFF_PHY</td><td>SENSE</td><td></td><td></td><td>REG_ISENVCC_3_NR 61 62</td></tr></table>				Electrical Constraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	Input Bus						1397	POWER	POWER	1.2V		PP12V_S0_CPUVCC FLT 61 62	1398	POWER	POWER	5V		REG_VCC_U7000 61	Local Ground						1399	GND	GND	0V		AGND_CPU 61 62 71	Phase 1						1400	VR_CTL_PHY	VR_CTL			REG_THWN_1 62	1401	VR_CTL_PHY	VR_CTL			REG_PWM_CPUVCC_1 61 62	1402	VR_CTL_PHY	VR_CTL			REG_PWM_CPUVCC_1_R 61	1403	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE	REG_PHASE_CPUVCC_1 62	1404	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE	REG_PHASE_CPUVCC1 62	1405	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE	REG_BOOT_CPUVCC_1 62	1406	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE	REG_BOOT_CPUVCC_1_RC 62	1407	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE	REG_SNUBBER_CPUVCC_1 62	1408	POWER	POWER	1.8V		PPCPUVCC_S0_SENSE_1 62	1409	SNS_DIFF_PHY	SENSE			REG_ISENVCC_1_P 61 62	1410	SNS_DIFF_PHY	SENSE			REG_ISENVCC_1_N 62	1411	SNS_DIFF_PHY	SENSE			REG_ISENVCC_1_NR 61 62	Phase 2						1412	VR_CTL_PHY	VR_CTL			REG_THWN_2 62	1413	VR_CTL_PHY	VR_CTL			REG_PWM_CPUVCC_2 61 62	1414	VR_CTL_PHY	VR_CTL			REG_PWM_CPUVCC_2_R 61	1415	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE	REG_PHASE_CPUVCC_2 62	1416	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE	REG_PHASE_CPUVCC2 62	1417	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE	REG_BOOT_CPUVCC_2 62	1418	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE	REG_BOOT_CPUVCC_2_RC 62	1419	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE	REG_SNUBBER_CPUVCC_2 62	1420	POWER	POWER	1.8V		PPCPUVCC_S0_SENSE_2 62	1421	SNS_DIFF_PHY	SENSE			REG_ISENVCC_2_P 61 62	1422	SNS_DIFF_PHY	SENSE			REG_ISENVCC_2_N 62	1423	SNS_DIFF_PHY	SENSE			REG_ISENVCC_2_NR 61 62	Phase 3						1424	VR_CTL_PHY	VR_CTL			REG_THWN_3 62	1425	VR_CTL_PHY	VR_CTL			REG_PWM_CPUVCC_3 61 62	1426	VR_CTL_PHY	VR_CTL			REG_PWM_CPUVCC_3_R 61	1427	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE	REG_PHASE_CPUVCC_3 62	1428	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE	REG_PHASE_CPUVCC3 62	1429	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE	REG_BOOT_CPUVCC_3 62	1430	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE	REG_BOOT_CPUVCC_3_RC 62	1431	VR_CTL_PHY	VR_SWITCH	1.2V	TRUE	REG_SNUBBER_CPUVCC_3 62	1432	POWER	POWER	1.8V		PPCPUVCC_S0_SENSE_3 62	1433	SNS_DIFF_PHY	SENSE			REG_ISENVCC_3_P 61 62	1434	SNS_DIFF_PHY	SENSE			REG_ISENVCC_3_N 62	1435	SNS_DIFF_PHY	SENSE			REG_ISENVCC_3_NR 61 62	<table><tr><th>Electrical Constraint Set</th><th>Physical</th><th>Spacing</th><th>Voltage</th><th>DIDT</th><th>NO_TEST</th></tr><tr><td colspan="6">ISL6372</td></tr><tr><td>1436</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_CPUVCC_DVC 61</td></tr><tr><td>1437</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>CPUVCC_DVC_RC 61</td></tr><tr><td>1438</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>CPUVCC_FB_RC_2 61</td></tr><tr><td>1439</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_CPUVCC_COMP 61</td></tr><tr><td>1440</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>CPUVCC_COMP_RC 61</td></tr><tr><td>1441</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_CPUVCC_FB 61</td></tr><tr><td>1442</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>CPUVCC_FB_RC 61</td></tr><tr><td>1443</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>CPUVCC_FB_R_1 61</td></tr><tr><td>1444</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>CPUVCC_FB_R_2 61</td></tr><tr><td>1445</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>CPUVCC_PSICOMP_RC 61</td></tr><tr><td>1446</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_CPUVCC_PSICOMP 61</td></tr><tr><td>1447</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_CPUVCC_HFCOMP 61</td></tr><tr><td>1448</td><td>SNS_DIFF_PHY</td><td>SENSE</td><td></td><td></td><td>CPU_VCCSENSE_P 8 61</td></tr><tr><td>1449</td><td>SNS_DIFF_PHY</td><td>SENSE</td><td></td><td></td><td>CPU_VCCSENSE_N 9 61</td></tr><tr><td>1450</td><td>SNS_DIFF_PHY</td><td>SENSE</td><td></td><td></td><td>CPU_VCCSENSE_R_P 61</td></tr><tr><td>1451</td><td>SNS_DIFF_PHY</td><td>SENSE</td><td></td><td></td><td>CPU_VCCSENSE_R_N 61</td></tr><tr><td>1452</td><td>SNS_DIFF_PHY</td><td>SENSE</td><td>0.5V</td><td></td><td>SNS_VCC_XW_P 61</td></tr><tr><td>1453</td><td>SNS_DIFF_PHY</td><td>SENSE</td><td>0.5V</td><td></td><td>SNS_VCC_XW_N 61</td></tr><tr><td>1454</td><td></td><td>SENSE</td><td></td><td></td><td>REG_CPUVCC_VSEN 61</td></tr><tr><td>1455</td><td></td><td>SENSE</td><td></td><td></td><td>REG_CPUVCC_RGND 61</td></tr><tr><td>1456</td><td></td><td>SENSE</td><td></td><td></td><td>REG_CPUVCC_VIN 61</td></tr><tr><td>1457</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_CPUVCC_IMON 48 61</td></tr><tr><td>1458</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>CPUVCC_IMON_R 61</td></tr><tr><td>1459</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_CPUVCC_TM 61</td></tr><tr><td>1460</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_CPUVCC_IMX 61</td></tr><tr><td>1461</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_CPUVCC_NPSI 61</td></tr><tr><td>1462</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_CPUVCC_FDVID 61</td></tr><tr><td>1463</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_CPUVCC_TMX 61</td></tr><tr><td>1464</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_CPUVCC_MEMVRSEL 61</td></tr><tr><td>1465</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td>REG_CPUVCC_RSET 61</td></tr><tr><td>1466</td><td>CPU_VIDSCLK</td><td>VR_VID_PHY</td><td>VR_VID</td><td></td><td>CPU_VIDSCLK 8 61</td></tr><tr><td>1467</td><td></td><td>VR_VID_PHY</td><td>VR_VID</td><td></td><td>CPU_VIDSCLK_R 8</td></tr><tr><td>1468</td><td>CPU_VIDALERT_L</td><td>VR_VID_PHY</td><td>VR_VID</td><td></td><td>CPU_VIDALERT_L 8 61</td></tr><tr><td>1469</td><td></td><td>VR_VID_PHY</td><td>VR_VID</td><td></td><td>CPU_VIDALERT_R_L 8</td></tr><tr><td>1470</td><td>CPU_VIDSOUT</td><td>VR_VID_PHY</td><td>VR_VID</td><td></td><td>CPU_VIDSOUT 8 61</td></tr><tr><td>1471</td><td></td><td>VR_VID_PHY</td><td>VR_VID</td><td></td><td>CPU_VIDSOUT_R 8</td></tr><tr><td colspan="6">Output Bus</td></tr><tr><td>1472</td><td>POWER</td><td>POWER</td><td>1.8V</td><td></td><td>PPCPUVCC_S0_CPU 70</td></tr></table>				Electrical Constraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	ISL6372						1436	VR_CTL_PHY	VR_CTL			REG_CPUVCC_DVC 61	1437	VR_CTL_PHY	VR_CTL			CPUVCC_DVC_RC 61	1438	VR_CTL_PHY	VR_CTL			CPUVCC_FB_RC_2 61	1439	VR_CTL_PHY	VR_CTL			REG_CPUVCC_COMP 61	1440	VR_CTL_PHY	VR_CTL			CPUVCC_COMP_RC 61	1441	VR_CTL_PHY	VR_CTL			REG_CPUVCC_FB 61	1442	VR_CTL_PHY	VR_CTL			CPUVCC_FB_RC 61	1443	VR_CTL_PHY	VR_CTL			CPUVCC_FB_R_1 61	1444	VR_CTL_PHY	VR_CTL			CPUVCC_FB_R_2 61	1445	VR_CTL_PHY	VR_CTL			CPUVCC_PSICOMP_RC 61	1446	VR_CTL_PHY	VR_CTL			REG_CPUVCC_PSICOMP 61	1447	VR_CTL_PHY	VR_CTL			REG_CPUVCC_HFCOMP 61	1448	SNS_DIFF_PHY	SENSE			CPU_VCCSENSE_P 8 61	1449	SNS_DIFF_PHY	SENSE			CPU_VCCSENSE_N 9 61	1450	SNS_DIFF_PHY	SENSE			CPU_VCCSENSE_R_P 61	1451	SNS_DIFF_PHY	SENSE			CPU_VCCSENSE_R_N 61	1452	SNS_DIFF_PHY	SENSE	0.5V		SNS_VCC_XW_P 61	1453	SNS_DIFF_PHY	SENSE	0.5V		SNS_VCC_XW_N 61	1454		SENSE			REG_CPUVCC_VSEN 61	1455		SENSE			REG_CPUVCC_RGND 61	1456		SENSE			REG_CPUVCC_VIN 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1462	VR_CTL_PHY	VR_CTL			REG_CPUVCC_FDVID 61																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																
1463	VR_CTL_PHY	VR_CTL			REG_CPUVCC_TMX 61																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																
1464	VR_CTL_PHY	VR_CTL			REG_CPUVCC_MEMVRSEL 61																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																
1465	VR_CTL_PHY	VR_CTL			REG_CPUVCC_RSET 61																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																
1466	CPU_VIDSCLK	VR_VID_PHY	VR_VID		CPU_VIDSCLK 8 61																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																
1467		VR_VID_PHY	VR_VID		CPU_VIDSCLK_R 8																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																
1468	CPU_VIDALERT_L	VR_VID_PHY	VR_VID		CPU_VIDALERT_L 8 61																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																
1469		VR_VID_PHY	VR_VID		CPU_VIDALERT_R_L 8																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																
1470	CPU_VIDSOUT	VR_VID_PHY	VR_VID		CPU_VIDSOUT 8 61																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																
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1472	POWER	POWER	1.8V		PPCPUVCC_S0_CPU 70																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																
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SYNC MASTER=J16 ROSSANA

SYNC DATE=12/14/2012





CPU VReg Constraints

 Apple Inc.

DRAWING NUMBER
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REVISION
12.4.0

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12V					
Physical	Spacing	Voltage	D1D2	NO_TEST	
Input Bus					
 POWER	POWER	12V			PP12V ACDC
FET Switched					
 POWER	POWER	12V			PP12V S5
 POWER	POWER	12V			PP12V S0
Sensed					
 POWER	POWER	12V			PP12V G3H

Physical		Spacing	Voltage	DIDT	NO_TEST
3.42V G3H					
HE40	POWER	VR_SWITCH	1.2V	TRUE	P3V42G3H_BOOST
HE40	POWER	VR_SWITCH	1.2V	TRUE	P3V42G3H_SW
HE40	VR_CTL_RHY	VR_CTL			P3V42G3H_FB
HE40	VR_CTL_RHY	VR_CTL			P3V42G3H_SHDN_L
Output Bus					
HE40	POWER	POWER	3.425V		PP3V42_G3H

3.3V G3					
Physical	Spacing	Voltage	DIDT	NO_TEST	
PP3V3	POWER	POWER	3.3V		PP3V3_G3

Physical	Spacing	Voltage	DIDT	NO_TEST
Input Bus				
POWER	POWER	12V		REG VIN U7600
POWER	POWER	5V		REG VCC1 U7600
POWER	POWER	5V		REG VCC2 U7600
3.3V S5				
VR_DIDT_PHV	VR_SWITCH	12V	TRUE	REG PHASE P3V3S5
VR_DIDT_PHV	VR_SWITCH	12V	TRUE	REG BOOT P3V3S5
VR_DIDT_PHV	VR_SWITCH	12V	TRUE	REG BOOT P3V3S5 RC
VR_DIDT_PHV	VR_SWITCH	12V	TRUE	REG UGATE P3V3S5
VR_DIDT_PHV	VR_SWITCH	12V	TRUE	REG LGATE P3V3S5
VR_DIDT_PHV	VR_SWITCH	12V	TRUE	REG SNUBBER P3V3S5
VR_CTL_PHV	VR_CTL			REG P3V3S5 ISEN
VR_CTL_PHV	VR_CTL			REG P3V3S5 OCSET
VR_CTL_PHV	VR_CTL			REG P3V3S5 FSET
VR_CTL_PHV	VR_CTL			REG P3V3S5 VOUT
VR_CTL_PHV	VR_CTL			REG P3V3S5 VOUT R
VR_CTL_PHV	VR_CTL			REG P3V3S5 FB
5V S3				
VR_DIDT_PHV	VR_SWITCH	12V	TRUE	REG PHASE P5V54
VR_DIDT_PHV	VR_SWITCH	12V	TRUE	REG BOOT P5V54
VR_DIDT_PHV	VR_SWITCH	12V	TRUE	REG BOOT P5V54 RC
VR_DIDT_PHV	VR_SWITCH	12V	TRUE	REG UGATE P5V54
VR_DIDT_PHV	VR_SWITCH	12V	TRUE	REG LGATE P5V54
VR_DIDT_PHV	VR_SWITCH	12V	TRUE	REG SNUBBER P5V54
VR_CTL_PHV	VR_CTL			REG P5V54 ISEN
VR_CTL_PHV	VR_CTL			REG P5V54 OCSET
VR_CTL_PHV	VR_CTL			REG P5V54 FSET
VR_CTL_PHV	VR_CTL			REG P5V54 VOUT
VR_CTL_PHV	VR_CTL			REG P5V54 VOUT R
VR_CTL_PHV	VR_CTL			REG P5V54 FB
Output Bus				
POWER	POWER	5V		PP5V_S5
POWER	POWER	5V		PP5V_S4
POWER	POWER	3.3V		PP3V3_S5
FET Switched				
POWER	POWER	5V		PP5V_S0
POWER	POWER	3.3V		PP3V3_S4
POWER	POWER	3.3V		PP3V3_S0
POWER	POWER	3.3V		PP3V3_S0 SSD
POWER	POWER	3.3V		PP3V3_ENET
POWER	POWER	3.3V		PP3V3_TBTLIC
Sensed				
POWER	POWER	3.3V		PPSSD_S0
POWER	POWER	3.3V		PP3V3_S4 AP

HDD S0					
Physical	Spacing	Voltage	DIDT	NO_TEST	
FET Switched					
R335 POWER	POWER	5V			PPHDD S0
Sensed					
R140 POWER	POWER	5V			PP5V S0 HDD

LV5 S0					
Physical		Spacing	Voltage	DIDT	NO_TEST
OUTPUT BUS					
R149	PWRER	PWRER	1.5V		PPIV5_S0
R135	VR_CTT_PHV	VR_CTT			REG_PIV5S0_SS
R140	VR_CTT_PHV	VR_CTT			REG_PIV5S0_ISET
R149	VR_CTT_PHV	VR_CTT			REG_PIV5S0_ADJ

Ground/Common					
Physical	Spacing	Voltage	DIDT	NO_TEST	
Common GND	GND	0V			GND

Thunderbolt

Thunderbolt-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBTDP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Thunderbolt-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C	*	=2x_DIELECTRIC	?
TBT_SPI	*	=2x_DIELECTRIC	?
TBTDP	*	=5x_DIELECTRIC	?
TBTDP	TOP, BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

DisplayPort

DP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

DP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

Pairs should be within 100 mils of clock length.

Max length of DisplayPort traces: 12 inches

DisplayPort intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.

DisplayPort AUX channel intra-pair matching should be 5 ps. No relationship to other signals.

TBT IC Net Properties

Electrical Constraint Set	Physical	Spacing		
689	DE_85D	DISPLAYBORT	DP_TBTSNK0 ML C P<3..0>	26 71
690	DE_85D	DISPLAYBORT	DP_TBTSNK0 ML C N<3..0>	26 71
691 DE_TBTSNK0_ML	DE_85D	DISPLAYBORT	DP_TBTSNK0 ML P<3..0>	26
692 DE_TBTSNK0_ML	DE_85D	DISPLAYBORT	DP_TBTSNK0 ML N<3..0>	26
693	DE_85D	DISPLAYBORT	DP_TBTSNK0 AUXCH C P	26 71
694	DE_85D	DISPLAYBORT	DP_TBTSNK0 AUXCH C N	26
695 DE_TBTSNK0_AUX	DE_85D	DISPLAYBORT	DP_TBTSNK0 AUXCH P	26
696 DE_TBTSNK0_AUX	DE_85D	DISPLAYBORT	DP_TBTSNK0 AUXCH N	26
697	DE_85D	DISPLAYBORT	DP_TBTSNK1 ML C P<3..0>	26 71
698	DE_85D	DISPLAYBORT	DP_TBTSNK1 ML C N<3..0>	26 71
699 DE_TBTSNK1_ML	DE_85D	DISPLAYBORT	DP_TBTSNK1 ML P<3..0>	26 71
700 DE_TBTSNK1_ML	DE_85D	DISPLAYBORT	DP_TBTSNK1 ML N<3..0>	26
701	DE_85D	DISPLAYBORT	DP_TBTSNK1 AUXCH C P	26 71
702	DE_85D	DISPLAYBORT	DP_TBTSNK1 AUXCH C N	26 71
703 DE_TBTSNK1_AUX	DE_85D	DISPLAYBORT	DP_TBTSNK1 AUXCH P	26
704 DE_TBTSNK1_AUX	DE_85D	DISPLAYBORT	DP_TBTSNK1 AUXCH N	26
705	DE_85D	DISPLAYBORT	DP_TBTSRC ML P<3..0>	41
706 DE_INTEN1_TB1_ML_MUX	DE_85D	DISPLAYBORT	DP_TBTSRC ML N<3..0>	41
707 DE_INTEN1_TB1_ML_MUX	DE_85D	DISPLAYBORT	DP_TBTSRC ML C P<3..0>	41
708 DE_INTEN1_TB1_ML_MUX	DE_85D	DISPLAYBORT	DP_TBTSRC ML C N<3..0>	41
709 DE_INTEN1_TB1_AUX_MUX	DE_85D	DISPLAYBORT	DP_TBTSRC AUXCH P	41
710 DE_INTEN1_TB1_AUX_MUX	DE_85D	DISPLAYBORT	DP_TBTSRC AUXCH N	41
711	DE_85D	DISPLAYBORT	DP_TBTSRC AUX C P	41
712	DE_85D	DISPLAYBORT	DP_TBTSRC AUX C N	41
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*: Only used on hosts supporting T29 video-in

DisplayPort

Electrical Constraint Set	Physical	Spacing	
Graphics Source			
DE_INTENL_DP_ML_MUX	DE_85D	DISPLAYPORT	DP INT ML P<1..0> 41 71
DE_INTENL_DP_ML_MUX	DE_85D	DISPLAYPORT	DP INT ML N<1..0> 41 71
DE_INTENL_Q0_AUX_MUX	DE_85D	DISPLAYPORT	DP INT AUX P 41 71
DE_INTENL_Q0_AUX_MUX	DE_85D	DISPLAYPORT	DP INT AUX N 41 71
	DE_85D	DISPLAYPORT	DP INT AUX C P 41 71
	DE_85D	DISPLAYPORT	DP INT AUX C N 41
Internal Panel			
	DE_85D	DISPLAYPORT	DP INTPNL MI_C P<3..0> 41
	DE_85D	DISPLAYPORT	DP INTPNL MI_C N<3..0> 41
DE_INTENL_MI_CONN	DE_85D	DISPLAYPORT	DP INTPNL MI_P<3..0> 40 41
DE_INTENL_MI_CONN	DE_85D	DISPLAYPORT	DP INTPNL MI_N<3..0> 40 41
DE_INTENL_AUX_CONN	DE_85D	DISPLAYPORT	DP INTPNL AUX P 40 41
DE_INTENL_AUX_CONN	DE_85D	DISPLAYPORT	DP INTPNL AUX N 40 41
Internal DP SPDIF			
		HDA	DP INT SPDIF AUDIO 40 52

TBT/DP Net Properties

Electrical Constraint Set		Physical	Spacing	
Port A				
EQ401	TBT_A R2D1	TBTDP_90D	TBTDP	TBT_A R2D C P<1>
EQ402	TBT_A R2D1	TBTDP_90D	TBTDP	TBT_A R2D C N<1>
EQ403	TBT_A R2D0	TBTDP_90D	TBTDP	TBT_A R2D C P<0>
EQ404	TBT_A R2D0	TBTDP_90D	TBTDP	TBT_A R2D C N<0>
EQ405		TBTDP_90D	TBTDP	TBT_A R2D P<1..0>
EQ406		TBTDP_90D	TBTDP	TBT_A R2D N<1..0>
EQ407	DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML C P<1>
EQ408	DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML C N<1>
EQ409	DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML C P<3>
EQ410	DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML C N<3>
EQ411		DP_85D	DISPLAYPORT	DP_TBTPA_ML P<1>
EQ412		DP_85D	DISPLAYPORT	DP_TBTPA_ML N<1>
EQ413		DP_85D	DISPLAYPORT	DP_TBTPA_ML P<3>
EQ414		DP_85D	DISPLAYPORT	DP_TBTPA_ML N<3>
EQ415	DP_A_LSX	DP_85D	DISPLAYPORT	DP_A LSX ML P<1>
EQ416	DP_A LSX	DP_85D	DISPLAYPORT	DP_A LSX ML N<1>
EQ417		TBTDP_90D	TBTDP	TBT_A D2R C P<1..0>
EQ418		TBTDP_90D	TBTDP	TBT_A D2R C N<1..0>
EQ419	TBT_A D2R1	TBTDP_90D	TBTDP	TBT_A D2R P<1>
EQ420	TBT_A D2R1	TBTDP_90D	TBTDP	TBT_A D2R N<1>
EQ421	TBT_A D2R0	TBTDP_90D	TBTDP	TBT_A D2R P<0>
EQ422	TBT_A D2R0	TBTDP_90D	TBTDP	TBT_A D2R N<0>
EQ423	TBT_A AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH C P
EQ424	TBT_A AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH C N
EQ425		DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH P
EQ426		DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH N
EQ427	DP_A_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_A AUXCH DDC P
EQ428	DP_A_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_A AUXCH DDC N
EQ429		TBTDP_90D	TBTDP	TBT_A D2R1 AUXDDC_P
EQ430		TBTDP_90D	TBTDP	TBT_A D2R1 AUXDDC_N
Port B				
EQ431	TBT_B R2D1	TBTDP_90D	TBTDP	TBT_B R2D C P<1>
EQ432	TBT_B R2D1	TBTDP_90D	TBTDP	TBT_B R2D C N<1>
EQ433	TBT_B R2D0	TBTDP_90D	TBTDP	TBT_B R2D C P<0>
EQ434	TBT_B R2D0	TBTDP_90D	TBTDP	TBT_B R2D C N<0>
EQ435		TBTDP_90D	TBTDP	TBT_B R2D P<1..0>
EQ436		TBTDP_90D	TBTDP	TBT_B R2D N<1..0>
EQ437	DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML C P<1>
EQ438	DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML C N<1>
EQ439	DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML C P<3>
EQ440	DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML C N<3>
EQ441		DP_85D	DISPLAYPORT	DP_TBTPB_ML P<1>
EQ442		DP_85D	DISPLAYPORT	DP_TBTPB_ML N<1>
EQ443		DP_85D	DISPLAYPORT	DP_TBTPB_ML P<3>
EQ444		DP_85D	DISPLAYPORT	DP_TBTPB_ML N<3>
EQ445	DP_B LSX	DP_85D	DISPLAYPORT	DP_B LSX ML P<1>
EQ446	DP_B LSX	DP_85D	DISPLAYPORT	DP_B LSX ML N<1>
EQ447		TBTDP_90D	TBTDP	TBT_B D2R C P<1..0>
EQ448		TBTDP_90D	TBTDP	TBT_B D2R C N<1..0>
EQ449	TBT_B D2R1	TBTDP_90D	TBTDP	TBT_B D2R P<1>
EQ450	TBT_B D2R1	TBTDP_90D	TBTDP	TBT_B D2R N<1>
EQ451	TBT_B D2R0	TBTDP_90D	TBTDP	TBT_B D2R P<0>
EQ452	TBT_B D2R0	TBTDP_90D	TBTDP	TBT_B D2R N<0>
EQ453	TBT_B AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH C P
EQ454	TBT_B AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH C N
EQ455		DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH P
EQ456		DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH N
EQ457	DP_B_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_B AUXCH DDC P
EQ458	DP_B_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_B AUXCH DDC N
EQ459		TBTDP_90D	TBTDP	TBT_B D2R1 AUXDDC_P
EQ460		TBTDP_90D	TBTDP	TBT_B D2R1 AUXDDC_N

Backlight Controller

BLC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BLC_P6MM	*	Y	0.600 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD
BLC_P3MM	*	Y	0.300 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_BLC	*	BLC_P6MM
POWER_BLC_RET	*	BLC_P3MM
BLC_CTL_PHY	*	BLC_P3MM

BLC-specific Spacing Definitions

BLC High Voltage Output

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_HV_ISO	*	0.45mm	1000

BLC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PHASE_ISO	*	=8:1_SPACING	2000
PHASE_SW2SW	*	=1:1_SPACING	?
PHASE_SW2PWR	*	=2:1_SPACING	?
PHASE_SW2GND	*	=2:1_SPACING	?

BLC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_CTL_ISO	*	= 3 : 1_SPACING	?

Constraints

BLC High Voltage Output

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_HV	BLC_CTL	*	BLC_CTL_ISO
BLC_HV	BLC_HV	*	BLC_CTL_ISO
BLC_HV	*	*	BLC_HV_ISO

BLC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_PHASE	*	*	PHASE_ISO
BLC_PHASE	BLC_PHASE	*	PHASE_SW2SW
BLC_PHASE	POWER	*	PHASE_SW2PWR
BLC_PHASE	GND	*	PHASE_SW2GND

BLC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_CTL	*	*	BLC_CTL_ISO

Is it chel'oh or sel'oh?

Physical	Spacing	Voltage	DITD	NO_TEST
Input Bus				
POWER	POWER	12V		PP12V_BKLT_SNS
POWER	POWER	12V		PP12V_BKLT_FUSED
POWER	POWER	12V		PP12V_S0_BKLT_FILT
POWER	POWER	12V		PP12V_S0_BKLT_PWR
POWER	POWER	12V		PP12V_S0_BKLT_PWR_R
POWER	POWER	5V		PP5V_S0_BKLT_R
POWER	POWER	3.3V		PP3V3_S0_BKLT_VDDIO_R
Local Ground				
BLC_CTL_PHY	BLC_PHASE	0V		PGND_BKLT
BLC_CTL_PHY	BLC_PHASE	0V		DGND_BKLT
BLC_CTL_PHY	BLC_PHASE	0V		LGND_BKLT
Backlight				
POWER_BLC	BLC_PHASE	80V	TRUE	BKLT_PHASE
BLC_CTL_PHY	BLC_PHASE	80V	TRUE	BKLT_GATE
BLC_CTL_PHY	BLC_PHASE	80V	TRUE	BKLT_GATE_R
BLC_CTL_PHY	BLC_PHASE	80V	TRUE	BKLT_SNUBBER
BLC_CTL_PHY	BLC_PHASE	12V	TRUE	BKLT_SW_R
BLC_CTL_PHY	BLC_CTL			BKLT_ISET
BLC_CTL_PHY	BLC_CTL			BKLT_FLT
BLC_CTL_PHY	BLC_CTL			BKLT_FLT_RC
SNS_DIFF_PHY	SENSE			BKLT_SW_P
SNS_DIFF_PHY	SENSE			BKLT_SW_N
	SENSE			BKLT_FB
BLC_HV		67V		BKLT_FB_XW
BLC_HV		67V		BKLT_FB_R
POWER_BLC_RET	BLC_CTL			BKLT_ISEN1
POWER_BLC_RET	BLC_CTL			BKLT_ISEN2
POWER_BLC_RET	BLC_CTL			BKLT_ISEN3
POWER_BLC_RET	BLC_CTL			BKLT_ISEN4
POWER_BLC_RET	BLC_CTL			BKLT_ISEN5
POWER_BLC_RET	BLC_CTL			BKLT_ISEN6
POWER_BLC_RET	BLC_HV			BKLT_ISEN1_R
POWER_BLC_RET	BLC_HV			BKLT_ISEN2_R
POWER_BLC_RET	BLC_HV			BKLT_ISEN3_R
POWER_BLC_RET	BLC_HV			BKLT_ISEN4_R
POWER_BLC_RET	BLC_HV			BKLT_ISEN5_R
POWER_BLC_RET	BLC_HV			BKLT_ISEN6_R
POWER_BLC_RET	BLC_HV			LED_RETURN_1
POWER_BLC_RET	BLC_HV			LED_RETURN_2
POWER_BLC_RET	BLC_HV			LED_RETURN_3
POWER_BLC_RET	BLC_HV			LED_RETURN_4
POWER_BLC_RET	BLC_HV			LED_RETURN_5
POWER_BLC_RET	BLC_HV			LED_RETURN_6
Output Bus				
POWER_BLC	BLC_HV	67V		BKLT_BOOST
POWER_BLC	BLC_HV	67V		BKLT_BOOST_1
POWER_BLC	BLC_HV	67V		BKLT_BOOST_2

Cello Miscellaneous

Electrical Constraint Set	Physical	Spacing	
SPI			
	SMB_PHY	SMB	BKLT_SCL 60
	SMB_PHY	SMB	BKLT_SDA 60